Contents

Syllabus

ELECTRONICS

SC–130

CHAPTER – 1 : CRYSTAL STRUCTURE AND DIFFRACTION

Crystalline and amorphous solids, Crystal structure, periodicity, lattice and bases, fundamental translation vectors, unit cell, Wigner-Seitz cell, symmetry operations, Bravais lattice in two and three dimensions sc, bcc and fcc lattice, lattice planes in a crystal, Miller indices and interplaner spacing, common crystal structures, NaCl, CsCl, Diamond and hcp.

X-Ray diffraction, Bragg's law, Laue method, Rotating Cylinder method and powder method for crystal structure.

CHAPTER – 2 : SOLID STATE DEVICES

Intrinsic semiconductors, electrons and holes, fermi level, temperature dependence of electron and hole concentration, Doping, impurity states, *n*- and *p*-type semiconductors, conductivity and mobility, *p-n* junction, majority and minority carriers, junction diode, Zener diode, tunnel diode, light emitting diode, photodiode, Schottky diode and solar cells.

Load line concept, half wave and full wave rectifiers, ripple factor and efficiency, filters, zener diode voltage regulator, IC voltage regulators.

CHAPTER – 3 : BIPOLAR TRANSISTOR

PNP and NPN transistor, working and characteristics of a transistor in CB, CE and CC mode, graphical analysis of CE configuration, low frequency equivalent circuits *h*-parameters, transistor biasing (fixed bias and voltage divider bias) and stabilization.

CHAPTER – 4 : FIELD EFFECT TRANSISTORS

Construction, working and Volt-ampere curves of JFET, a.c. operation of JFET, Depletion and enhancement mode MOSFET, biasing MOSFET, FET as variable voltage resistor Operational Amplifier (Op-app) Characteristics of Ideal Op-amp, parameter of Op-amp. Op-amp as inverting and non-inverting amplifier.

CHAPTER – 5 : SMALL SIGNAL AMPLIFIERS

General principles of operation, classification of amplifiers, R.C. coupled amplifiers, gain-frequency response, equivalent circuit at low, medium and high frequencies, input and output impedance, multistage amplifiers, transformer coupled amplifiers (qualitative analysis).

Low frequency common source and common drain amplifier, feedback in amplifiers, emitter follower and low frequency common source amplifier.

U N I T - I

CRYSTAL STRUCTURE AND DIFFRACTION

STRUCTURE

LEARNING OBJECTIVES

After learning this chapter, you will be able to know

- Study of crystals and amorphous solids.
- Different types of lattices in two dimension and three dimensions.
- Coordination numbers and atoms in different structures.
- Atomic radius and packing factor for different lattices.
- Study of h.c.p. structure.
- Study of NaCl, CsCl and diamond structure.
- Different methods of crystal structure determination.

1.1. DIFFERENCE BETWEEN CRYSTALS AND AMORPHOUS SOLIDS

Solids are of two types :

(i) Crystalline solids

(ii) Amorphous solids

(i) Crystalline solids : Most solids are crystalline. In these solids the arrangement of atoms, ions or molecules is regular and periodic. They show long range order in their structure. **Examples :** Calcite, quartz, rock salt etc.

(ii) Amorphous solids : In these solids the arrangement of atoms, ions or molecules is not regular and periodic. They show short-range order in their structure. **Examples :** Glass, plastic, wood etc.

The difference between two solids can be easily understood by considering the example of molecule B_2O_3. In the Fig. (1), amorphous B_2O_3 shows only short range order while crystalline B_2O_3 shows long-range order (Fig. 2).

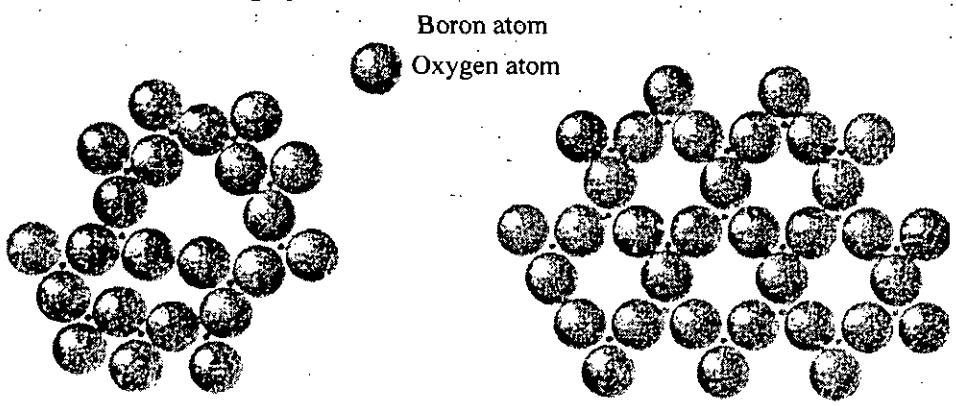


Fig. 1. Fig. 2

• 1.2. CRYSTALLOGRAPHY

A crystal is a three dimensional structure in which atoms are regularly and periodically arranged. If the crystal is struck into pieces then the arrangement of atoms remains unaffected. The study of these crystals is known as **"crystallography".**

Lattice : A lattice is a geometrical concept which is obtained by periodic arrangement of points in space. The structure of all crystals in described is terms of Lattice. Lattice may be defined as a regular and pentode arrangement of parts in crystals.

In the case of two dimension it is known as "plane lattice" and in the case of three dimension it is known as **space lattice".**

Translation vectors : Lattice is defined by three vectors $\vec{a}, \vec{b}, \vec{c}$ known as translation vectors. They are along the lattice axes X, Y, Z respectively. The location of any other atom can be written as :

$$\vec{T} = u\vec{a} + v\vec{b} + w\vec{c}$$

where u, v, w are arbitrary integers.

Basis : Each lattice is surrounded by a group of atoms. The group of such atoms is called **Basis.** Each basis is identical in composition, arrangement and orientation with any other basis. Hence crystal structure will be :

Lattice + basis = Crystal Structure

We can not pick the basis until we have selected the lattice and the axes.

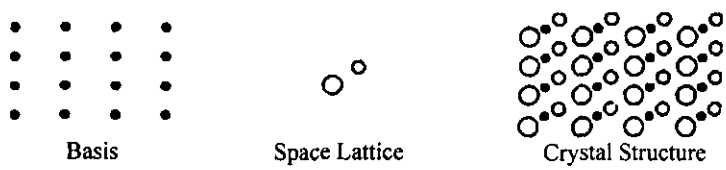


Fig. 3.

Unit cell : It is the smallest part of the crystal which is also three dimensional. The shape of the crystal depends upon the shape of the unit cell. It can be supposed to be the brick of the wall. As the shape of wall depends upon the shape of brick so the shape of crystal depends upon the shape of the unit cell. The translation vectors $\vec{a}, \vec{b}, \vec{c}$ are the

edges of the unit cell and they are also known as **primitives.** It is not necessary that all primitives be equal. α, β and γ are known as **interfacial angles** and *X*, *Y*, *Z* are known as **crystallographic axes.**

Primitive cell : It is defined as the smallest unit of volume of a crystal. It contains minimum number of atoms *i.e.*, the unit cell that contains one lattice part only at the corners is known as primitive cell. In some cases the two cells may coincide. The unit cell may be primitive cell, but all the primitive cells need not be the unit cell.

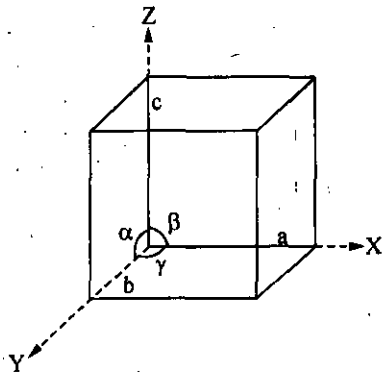


Fig. 4.

Lattice constant : The distance between two atoms in a unit cell is known as "lattice constant".

• 1.3. TWO DIMENSIONAL LATTICE TYPES

In a two dimensional lattice there is no restriction regarding the length of the primitives $\vec{a}$, and $\vec{b}$, and the angle ϕ between them. The only condition in two dimension is that the lattice should be invariant under symmetry operations.

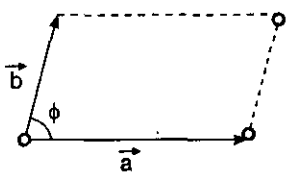


Fig. 5.

There are in all five types of lattice depending upon the values of $\vec{a}$, $\vec{b}$, and ϕ. These are known as **Bravais lattices** in two dimensions and are as under :

(i) Oblique lattice : A general lattice is known as oblique lattice and is invariant under rotation of 2π and $2\pi/2$. For this lattice $|\vec{a}| \neq |\vec{b}|$ and $\phi \neq 90°$. This type of lattice is shown in Figure 5. The conventional unit cell is a parallelogram.

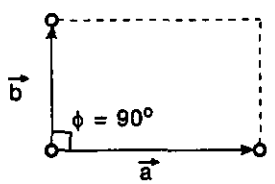


Fig. 6.

(ii) Square lattice : For this lattice $|\vec{a}| = |\vec{b}|$ and $\phi \neq 90°$. This lattice is shown in figure 6 and is invariant under a rotation of $2\pi/4$. The conventional unit cell is a square.

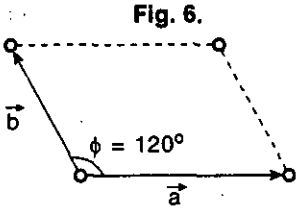


Fig. 7

(iii) Hexagonal lattice : For this lattice $|\vec{a}| = |\vec{b}|$ and $\phi = 120°$. This lattice is shown in figure 7 and is invariant under a rotation of $2\pi/6$. The conventional unit cell is a 60° rhombus.

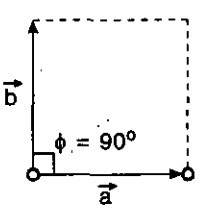


Fig. 8.

(iv) Primitive rectangular lattice : For this lattice $|\vec{a}| \neq |\vec{b}|$ and $\phi = 90°$. This lattice is shown in figure 8 and is invariant under mirror reflection. The conventional unit cell is a rectangle.

(v) Centred rectangular lattice : For this lattice $|\vec{a}| \neq |\vec{b}|$ and $\phi = 90°$ but $|\vec{a}| > |\vec{b}|$. This lattice is shown in figure 9 and is invariant under inversion operation. The conventional unit cell is a rectangle.

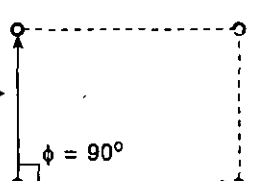


Fig. 9.

The two dimensional Bravais lattices in a tabular form are as under :

S. No.	Lattice	Crystal Axes	Conventional Unit Cell
1.	Oblique	$a \neq b$, $\phi \neq 90°$	Parallelogram
2.	Square	$a = b$, $\phi = 90°$	Square
3.	Hexagonal	$a = b$, $\phi = 120°$	60° Rhombus
4.	Primitive rectangular	$a = b$, $\phi = 90°$	Rectangle
5.	Centred rectangular	$a \neq b$ but $a, > b$, $\phi = 90°$	Rectangle

• 1.4. THREE DIMENSIONAL LATTICE TYPES

In three dimensional space lattices, there are fourteen types of lattices and are known as **Bravais space lattices.** On the basis of primitive cell, the crystals have been classified into seven systems. Figure 10 shows the lattice parameters a, b, c and the angles α, β, γ between them. There are following seven crystal systems in all :

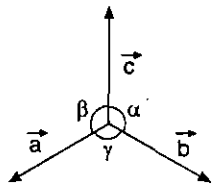


Fig. 10.

(i) Cubic crystals : In these crystals the length of the primitives is the same along the three axes *i.e.*, $\alpha = \beta = \gamma = 90°$. Cubic lattices may be simple (sc) or primitive (p), face

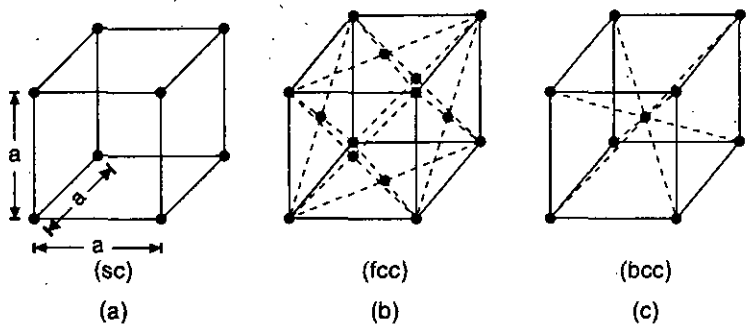


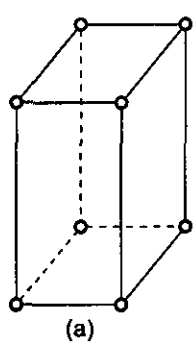
Fig. 11.

centred (fcc) or (F) and body centred (bcc) or (I) as shown in figure 11(a), (b) and (c).

(ii) Tetragonal crystals : In this type of crystals the lengths of the primitives along two axes are the same while the third axis is different, *i.e.*, $a = b \neq c$. The crystal axes are perpendicular to one another, *i.e.*, $\alpha = \beta = \gamma = 90°$. These crystals may be simple (P) or body centred (I) as shown in Figure 12 (a) and (b).

(iii) Hexagonal crystals : In this type of crystals two of the crystal axes are 120° apart, *i.e.*, $\gamma = 120°$ while the third is perpendicular to both of them, *i.e.*, $\alpha = \beta = 90°$. The lengths of the primitives are the same along the axes that are 120° (or 60°) apart but the third one is different, *i.e.*, $a = b \neq c$ as shoswn in figure 13.

(iv) Trigonal crystals : The crystals of this type are also known as rhombohedral. The lengths of primitives is same along the three axes, *i.e.*, $a = b = c$. The angle beween



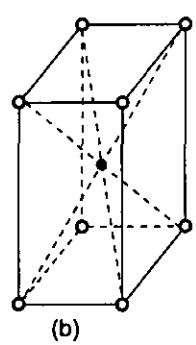


Fig. 12.

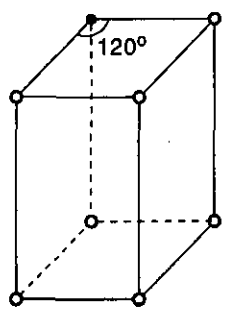


Fig. 13.

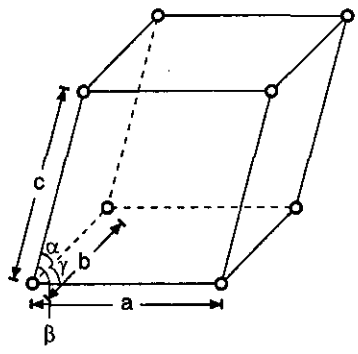


Fig. 14.

each pair of crystal axes are same but are not 90°, *i.e.*, $\alpha = \beta = \gamma \neq 90°$. The structure is shown in figure 14.

(v) Orthorhombic crystals : In this type of crystals the lengths of the primitives are different along all the three axes, *i.e.*, $a \neq b \neq c$. The crystal axes are perpendicular

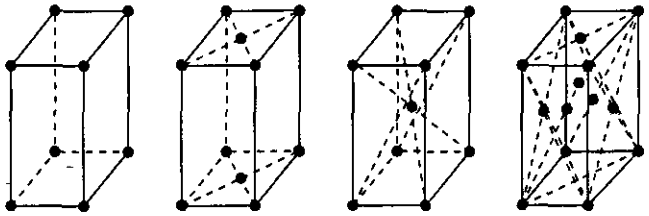


Fig. 15.

to one another. The crystal lattices may be simple, base centred, body centred or face centred as shown in figures 15 (a), (b), (c) and (d).

(vi) Monoclinic crystals : In this type of crystals the lengths of the primitives along the three axes are different, *i.e.*, $a \neq b \neq c$. Two crystal axes are not perpendicular to each other but the third is perpendicular to both of them. The lattices may be simple or base centred as shown in figure 16 (a) and (b).

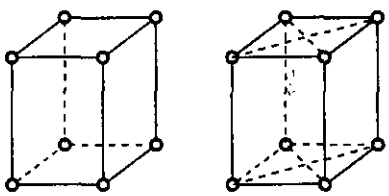


Fig. 16.

(vii) Triclinic crystals : In this type of crystals the length of all the three primitives is different, *i.e.*, $a \neq b \neq c$. None of the crystal axes is perpendicular to any of the others, *i.e.*, $\alpha \neq \beta \neq \gamma$. The crystal lattice is simple as shown in figure 17.

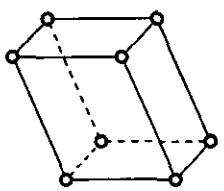


Fig. 17.

The class of crystals, types and number of lattices, length of primitives and angle between axes for all the 14 Bravais lattices is shown in the following table :

S. No.	Class of Crystal	Type and Number of Lattices	Length of the primitives	Angle between axes
1.	Cubic	sc, fcc, bcc (3)	$a = b = c$	$\alpha = \beta = \gamma = 90°$
2.	Tetragonal	sc, bcc (2)	$a = b \neq c$	$\alpha = \beta = \gamma = 90°$
3.	Hexagonal	sc (1)	$a = b \neq c$	$\alpha = \beta = 90°$, $\gamma = 120°$
4.	Trigonal (Rhombohedral)	sc (1)	$a = b = c$	$\alpha = \beta = \gamma \neq 90° < 120°$
5.	Orthorhombic	sc, fcc, bcc, base centred (4)	$a \neq b \neq c$	$\alpha = \beta = \gamma = 90°$
6.	Monoclinic	sc, base centred (2)	$a \neq b \neq c$	$\alpha = \beta = \gamma = 90° \neq \beta$
7.	Triclinic	sc (1)	$a \neq b \neq c$	$\alpha \neq \beta \neq \gamma$

• 1.5. ATOMS PER UNIT CELL

The study of cubic crystal lattice shows that :

(i) An atom lying at the corner of a cubic unit cell is shared equally by eight unit cells, hence counts for one eighth of an atom.

(ii) An atom lying on the face of a unit cell belongs equally to two unit cells and therefore counts as one half for that cell.

(iii) An atom lying completely within a unit cell belongs wholly to that cell.

Calculation of atoms per unit cell

(a) Simple cubic cell : In this cell there is one atom at each corner of the cell. Every atom is shared by eight unit cells. So each corner atom contributes only 1/8 of its effective part to a unit cell, as there are eight corners. Hence total contribution

$$= 8 \times \frac{1}{8} = 1.$$

Thus the number of atoms per unit simple cubic cell is 1.

(b) Face centred cubic cell : In this cell, in addition to eight corner atoms, there are six face centred atoms. Corner atom is shared by eight cells and each face centred atom is shared by two unit cells. Hence number of atoms in this cell are :

$$\frac{1}{8} \times 8 + \frac{1}{2} \times 6 = 1 + 3 = 4$$

Thus number of atoms per unit fcc cell are 4.

(c) Body centred cubic cell : In this cell, in addition to eight corner atoms, there is one body centred atom. Hence number of atoms per unit body centred cubic cell are :

$$\frac{1}{8} \times 8 + 1 = 1 + 1 = 2$$

Thus number of atoms per unit bcc cell are 2.

• 1.6. COORDINATION NUMBER

It is defined as the number of nearest neighbours around any lattice point or atom in the lattice.

(i) Coordination number for sc cell : Let us take any one of the lattice points as the origin and the three edges passing through that point as x, y and z-axes. The positions of the nearest neighbours of the origin are :

$$\pm a\,\hat{i}, \pm a\,\hat{j}, \pm a\,\hat{k}$$

as in simple cubic (sc) all the three sides of the lattice are equal *i.e.*, $a = b = c = a$ (let). The coordinates of the points stated above are :

$$(\pm a, 0, 0), (0, \pm a, 0), (0, 0, \pm a)$$

These are six in numbers. Hence the coordination number of a simple cubic cell is 6.

(ii) Coordination number of fcc cell : Let us take any one of the lattice points as the origin and the edges of the unit cell passing through that pint as x, y and z-axes. The positions of the nearest neighbours of the origin are :

$$\left(\pm \frac{a}{2}\hat{i} \pm \frac{a}{2}\hat{j}, \pm \frac{a}{2}\hat{j} \pm \frac{a}{2}\hat{k} \pm \frac{a}{2}\hat{k} \pm \frac{a}{2}\hat{i}\right)$$

The coordinates of these points are :

$$\left(\frac{a}{2}, \frac{a}{2}, 0\right), \left(-\frac{a}{2}, \frac{a}{2}, 0\right), \left(\frac{a}{2}, -\frac{a}{2}, 0\right), \left(-\frac{a}{2}, -\frac{a}{2}, 0\right),$$

$$\left(0, \frac{a}{2}, \frac{a}{2}\right), \left(0, -\frac{a}{2}, \frac{a}{2}\right), \left(0, \frac{a}{2}, -\frac{a}{2}\right), \left(0, -\frac{a}{2}, -\frac{a}{2}\right),$$

$$\left(\frac{a}{2}, 0, \frac{a}{2}\right), \left(\frac{a}{2}, 0, -\frac{a}{2}\right), \left(-\frac{a}{2}, 0, \frac{a}{2}\right), \left(-\frac{a}{2}, 0, -\frac{a}{2}\right).$$

These numbers are 12. Hence the coordination number of fcc cell is 12.

(iii) Coordination number of bcc cell : Let us take the lattice point at the body centre as the origin. x, y and z-axes being parallel to the edges of the unit cell. The positions of the nearest neighbours of the origin are :

$$\left(\pm\frac{a}{2}i, \pm\frac{a}{2}j, \pm\frac{a}{2}k\right)$$

The coordinates of these points are :

$$\left(\frac{a}{2},\frac{a}{2},\frac{a}{2}\right)\left(\frac{a}{2},\frac{a}{2},-\frac{a}{2}\right)\left(\frac{a}{2},-\frac{a}{2},\frac{a}{2}\right)\left(-\frac{a}{2},\frac{a}{2},\frac{a}{2}\right)$$

$$\left(\frac{a}{2},-\frac{a}{2},-\frac{a}{2}\right)\left(-\frac{a}{2},-\frac{a}{2},\frac{a}{2}\right)\left(-\frac{a}{2},\frac{a}{2},-\frac{a}{2}\right)\left(-\frac{a}{2},-\frac{a}{2},-\frac{a}{2}\right)$$

These numbers are 8. Hence the coordination number of bcc cell is 8.

• 1.7. ATOMIC RADIUS

It is supposed that all the atoms in a crystal have the same size and are touching each other. Thus, atomic radius is the distance between the centres of two neighbouring atoms.

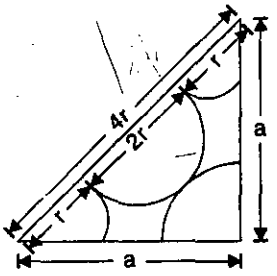


Fig. 8.

(i) Atomic radius for sc lattice : In case of sc lattice the lattice parameter is a. Let r be the atomic radius, then

$$a = 2r$$

or $$\boxed{r = a/2}$$

(ii) Atomic radius for fcc lattice : In fcc lattice the atoms are in contact along the diagonal of the faces as shown in figure 18.

Hence from figure,

$$(4r)^2 = a^2 + a^2 = 2a^2$$

or $$r = \frac{a^2}{8}$$

or $$\boxed{r = \frac{a}{2\sqrt{2}}}$$

(iii) Atomic radius for bcc lattice : In bcc lattice, the atoms touch each other along the diagonal of the cube as shown in figure 19.

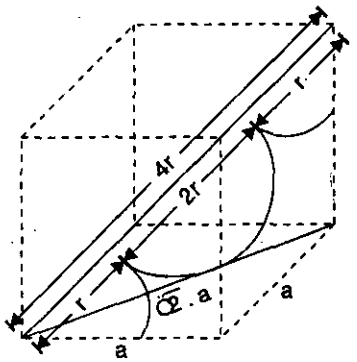


Fig. 19.

Hence from figure,

$$(4r)^2 = (\sqrt{2}a)^2 + a^2$$

$$= 2a^2 + a^2 = 3a^2$$

or $$r^2 = \frac{3}{16}a^2$$

or $$\boxed{r = \frac{\sqrt{3}}{4}a}$$

• 1.8. ATOMIC PACKING (OR FACTOR)

It is defined as the ratio of the volume of the atoms occupying the unit cell to the volume of the unit cell relating to the structure of the crystal.

(i) Packing factor for sc lattice : In a simple cubic (sc) structure the number of atoms per unit cell is one. The atomic radius is given by half the primitive.

i.e., $$r = \frac{a}{2}.$$

So, volume occupied by the atom in the unit cell

$$= \frac{4}{3}\pi r^3 = \frac{4}{3}\pi\left(\frac{a}{2}\right)^3$$

Volume of the unit cell $= a^3$

$$\therefore \quad \text{Packing factor } (f) = \frac{\frac{4}{3}\pi\left(\frac{a}{2}\right)^3}{a^3} = \frac{\pi}{6}.$$

(ii) Packing factor for fcc lattice : In fcc lattice the number of atoms per unit cell is four. The atomic radius

$$r = \frac{\sqrt{2}}{4}.a.$$

So, volume occupied by the atoms in the unit cell

$$= r \times \frac{4}{3}\pi r^3 = 4 \times \frac{4}{3}\pi\left(\frac{\sqrt{2}}{4}a\right)^3$$

$$= \frac{16}{3}\pi.\frac{2^{3/2}}{4^3}.a^3 = \frac{\pi}{3\sqrt{2}}.a^3$$

Volume of the unit cell $= a^3$

$$\therefore \quad \text{Packing factor } (f) = \frac{\frac{\pi}{3\sqrt{2}}.a^3}{a^3} = \frac{\pi}{3\sqrt{2}}.$$

(iii) Packing factor for bcc lattice: In bcc lattice there are two atoms per unit cell. The atomic radius is

$$r = \frac{\sqrt{3}}{4}.a.$$

So, volume occupied by the atoms in the unit cell

$$= 2 \times \frac{4}{3}\pi r^3 = 2 \times \frac{4}{3\pi}\left(\frac{\sqrt{3}}{4}a\right) = \frac{\sqrt{3}}{8}\pi a^3$$

Volume of the unit cell $= a^3$

$$\therefore \quad \text{Packing factor } (f) = \frac{\frac{\sqrt{3}}{8}\pi a^3}{a^3} = \frac{\sqrt{3}}{8}\pi.$$

• 1.9. LATTICE CONSTANT '*a*'

Given that M = Molecular weight

N = Avogadro's number

So mass of one molecule $= \frac{M}{N}$

Let n be the number of molecules per unit cell.

$$\text{So mass of unit cell} = \frac{nM}{N}$$

$$\text{density of the crystal, } \rho = \frac{m}{a^3} = \frac{nM}{Na^3}$$

or $$a^3 = \frac{nM}{\rho N}$$

or $$a = \left(\frac{nM}{N\rho}\right)^{1/3}$$

• 1.10. HEXAGONAL CLOSE PACKED STRUCTURE

If the constituent atoms of a crytal are arranged in such a manner that they occupy the least possible volume, the structure is called **Close Packed.**

Such type of structure occurs when the bonding forces are spherically symmetric as in inert gases.

Let us consider identical spheres and arrange them in a single closest packed layer by placing each sphere in contact with six others as shown in figure 20. The layer assumes hexagonal shape. A second layer identical to first can be formed over first by placing spheres on the hollows *B*, each formed by three spheres in the bottom layer. A third layer can be made in two ways.

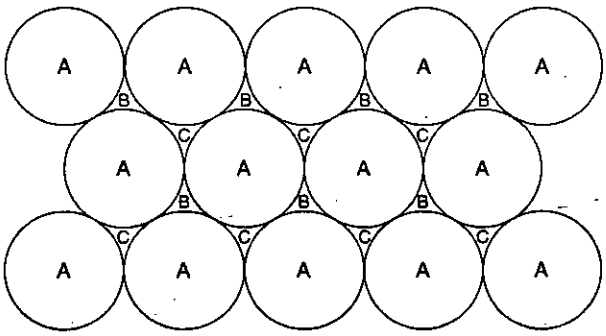


Fig. 20.

(i) The spheres in the third layer can be put over the hollows *C*. The position of spheres in successive layers is thus identical as *ABC, ABC,* .... This is the face centred cubic (fcc) structure.

(ii) The spheres in the third layer can be placed directly over the sphere placed in first layer. The position of spheres in successive layers of this structure may be indicated as *AB, AB, AB,*... . This leads to hexagonal close packed structure as shown in figure 21.

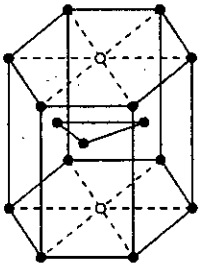


Fig. 21.

The coordination number in a close packed crystal (either fcc or hcp) is 12. The number of atoms present in a hexagonal cell is eight at the corners and one inside.

So number of atoms per unit cell $= 1 + \frac{1}{8} \times 8 = 2$

The base is a parallelogram with each side = a and angle between sides = 60° as shown in figure 22.

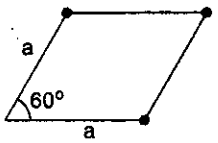


Fig. 22.

Hence area of the base $= a \times a \sin 60^\circ$

$$= \frac{a^2}{2} . \sqrt{3}$$

Volume of the hexagonal cell $= \frac{a^2}{2} . \sqrt{3}$

$$= \frac{a^2}{2} \sqrt{3} \times \frac{2a\sqrt{2}}{\sqrt{3}}$$

$$= a^3 . \sqrt{2}$$

Radius of the atom, $r = \frac{a}{2}$

Volume occupied by the atoms $= 2 \times \frac{4}{3} \pi r^3 = 2 \times \frac{4}{3} \pi \times \frac{a^3}{8} = \frac{\pi a^3}{3}$

So packing fraction $= \frac{\pi a^3 / 3}{a^3 . \sqrt{2}} = \frac{\pi}{3\sqrt{2}} = 0.74 = 74\%.$

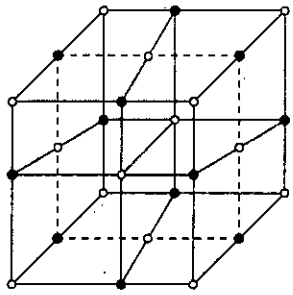
• 1.11. STRUCTURE OF CsCl

The structure of CsCl is shown in the Fig. 23. It is simple lattice. Value of cell is a^3, the co-ordination number is 8 and the distance between two nearest neighbours is 'a'.

• 1.12. SODIUM CHLORIDE STRUCTURE

In NaCl, Na atom loses its outer electron and acquires an excess positive charge. The Cl atom acquires the electron lost by Na atom and thus acquires an excess negative charge. In this way, we get Na^+ and Cl^- ions. These ions are arranged alternately in a cubic pattern in space so that the electrostatic attraction between Na^+ and Cl^- ions is maximum. Figure 24 shows a unit cell of NaCl lattice. The Na^+ ions are situated at the corners as well as at the centres of the faces of the cube. Cl^- ions have their same lattice being relatively displaced half the edge of the unit cell along each axis. Thus NaCl is an example of fcc Bravais lattice.s

Fig. 23.



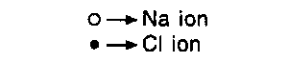


Fig. 24.

Coordinates of the atoms : In NaCl crystal the basis consists of one Na^+ ion and one Cl^- ion separated by one-half the body diagonal of a unit cube. There are four NaCl molecules in a unit cube in the positions whose coordinates are given below :

$$Na^+ \rightarrow 0\,0\,0, \frac{1}{2}\frac{1}{2}0, \frac{1}{2}0\frac{1}{2}0\frac{1}{2}\frac{1}{2}$$

$$Cl^- \rightarrow \frac{1}{2}\frac{1}{2}\frac{1}{2}, 0\,0\frac{1}{2}, 0\frac{1}{2}0, \frac{1}{2}00$$

Number of Na^+ ions in a unit cell : NaCl cubic lattice can be considered to be made up of two fcc sub lattices, one of Na^+ ions having origin at point (0 0 0) and the other of Cl^- ions having the origin mid way along the cube edge, *i.e.*, at point

$$\left[\frac{a}{2}, 0, 0\right].$$

Each Na^+ ion has 6 Cl^- as nearest neighbours and similarly each Cl^- ion has 6 Na^+ ions. Hence the coordination number of NaCl is 6.

The other crystals, which have the same structure, are PbS, KCl, KBr etc.

• 1.13. DIAMOND STRUCTURE

The space lattice of diamond is fcc with a basis of two carbon atoms at (0, 0, 0) and $\left(\frac{1}{4}, \frac{1}{4}, \frac{1}{4}\right)$ associated with each lattice point.

A two dimensional view of diamond cell is shown in figure 25. Fractions denote height above the base in fractions of cube edge. The points 0 and $\frac{1}{2}$ are on the fcc lattice. The points at $\frac{1}{4}$ and $\frac{3}{4}$ are on a similar lattice displaced along the body diagonal by $\frac{1}{4}$ of its length.

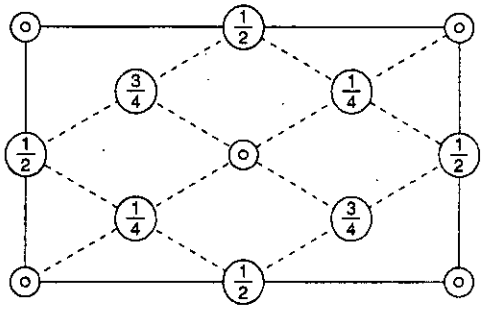


Fig. 25.

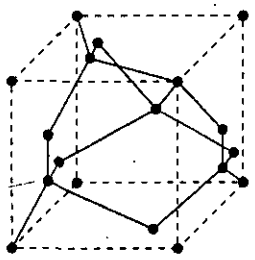


Fig. 26.

The three dimensional picture is obtained by inserting one fcc lattice into another fcc lattice displaced along the space diagonal by a quarter of its length. In this way, a corner atom of one fcc comes in contact with a corner atom of second fcc and not with an atom in a face. Each atom of one cube may, therefore, be regarded to be at the centre of a tetrahedron formed by four nearest neighbours belonging to the other cube. Thus each atom in a diamond structure forms four covalent bonds with its four nearest neighbours. The bond length is 1.544Å. The crystal structure of diamond showing the tetrahedral bond arrangement is shown in figure 26. Each atom has four nearest neighbours. Hence, the coordination number of diamond crystal is 4.

Packing fraction : The body diagonal of diamond is $8r$ as there are 3 full spheres and two half spheres on it. If a is the side of the cube, then

$$(8r)^2 = 3a^2$$

or $$r = \frac{\sqrt{3}}{8} . a$$

Volume occupied by the atoms in the unit cell

$$= 8 \times \frac{4}{3} \pi r^3$$

$$= 8 \times \frac{4}{3} \times \pi \times \frac{3\sqrt{3}}{8^3} . a^3$$

$$= \frac{\sqrt{3}}{16} \pi a^3$$

Volume of the unit cell $= a^3$

$$\therefore \quad \text{Packing fraction } (f) = \frac{\frac{\sqrt{3}}{16} \pi a^3}{a^3}$$

$$= \frac{\sqrt{3}}{16} \pi$$

$$= 0.34$$

$$= 34\%$$

• 1.14. MILLER INDICES

The position and orientation of a lattice plane in a crystal can be determined by three smallest whole numbers which have same ratios with one another as the reciprocals of the intercepts of the plane on the three crystal axes. These numbers denoted by h, k, l are known as Miller Indices of that plane. The following rules are applied to specify the orientation of a plane in crystal structure analysis :

(i) Find the intercepts of the plane on the crystal axes $\vec{a}$ $\vec{b}$ and $\vec{c}$ in terms of the lattice constant. The axes may be primitive or non-primitive.

(ii) Take the reciprocals of these numbers and then reduce to the smallest three integers having the same ratio. Denote the result as (h, k, l) enclosed in parentheses.

Orientation of a plane by Miller indices : Miller indices (h, k, l) may denote a single plane or a set of parallel planes. If a plane cuts an axis on the negative side of the origin, the index is denoted by placing a minus (–) sign above it. If the plane cuts an axis at infinity, the corresponding index is zero.

Let PQR be a standard plane cutting all the three axes at P, Q and R with intercepts OP, OQ and OR equal to a, b and c respectively, where $\vec{a}$ $\vec{b}$ and $\vec{c}$ are the translation

vectors of the crystal lattice. OX, OY and OZ are three axes parallel to the crystal axes as shown in figure 27.

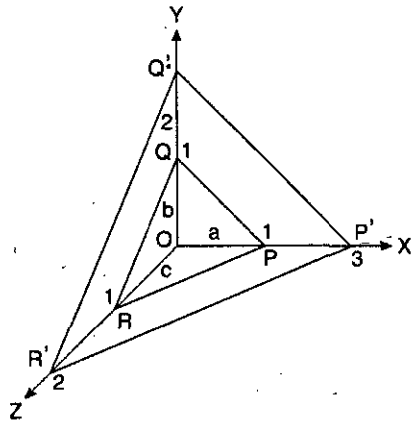


Fig. 27.

The directions of other faces of the crystal are governed by the law of rational indices, which states that a face parallel to a plane, whose intercepts on the three axes are m_1a, m_2b and m_3c where m_1, m_2 and m_3 are small whole numbers, is a possible face of the crystal. Thus if $P'Q'R'$ be a possible crystal face, then

$$OP' : OQ' : OR' = m_1a : m_2b : m_3c$$

$$= \frac{a}{m_2m_3} : \frac{b}{m_1m_3} : \frac{c}{m_1m_2}$$

$$= \frac{a}{h} : \frac{b}{k} : \frac{c}{l}$$

where $m_2m_3 = h, m_1m_3 = k, m_1m_2 = l$ are again small whole numbers. The numbers h, k, l are the Miller indices of the plane $P'Q'R'$ with respect to the standard plane PQR. The Miller indices of standard plane are always (1, 1, 1).

• 1.15. INTERPLANAR SPACING

Let us consider a simple unit cell in which the crystal axes $\vec{a}$ $\vec{b}$ and $\vec{c}$ are orthogonal and coincide with coordinate axes X, Y and Z respectively with O as origin taken at a lattice point. A plane ABC having Miller indices (h, k, l) have intercepts $\frac{a}{h}, \frac{b}{k}$ and $\frac{c}{l}$ as X, Y and Zaxes respectively. Draw ON perpendicular from O on the plane ABC. Let $ON = d$(figure 28). Also let ON make angles α, β and γ with X, Y and Z axes respectively. *According to law of direction cosines.*

$$\cos^2\alpha + \cos^2\beta + \cos^2\gamma = 1$$

From figure,

$$\frac{ON}{OA} = \cos\alpha$$

$$\frac{ON}{OB} = \cos\beta$$

$$\frac{ON}{OC} = \cos\gamma$$

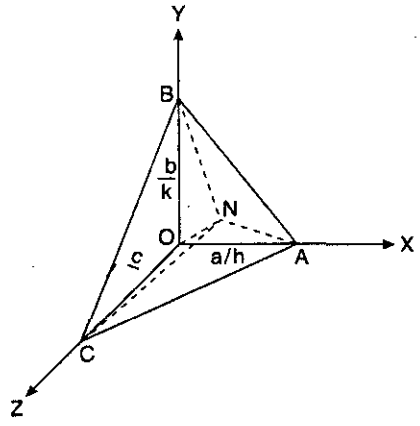


Fig. 28.

Hence $$\left(\frac{ON}{OA}\right)^2 + \left(\frac{ON}{OB}\right)^2 + \left(\frac{ON}{OC}\right)^2 = 1$$

or $$\left(\frac{d}{a/h}\right)^2 + \left(\frac{d}{b/k}\right)^2 + \left(\frac{d}{c/l}\right)^2 = 1$$

$$d^2\left[\frac{h^2}{a^2} + \frac{k^2}{b^2} + \frac{l^2}{c^2}\right] = 1$$

or $$d^2 = \frac{1}{\left[\frac{h^2}{a^2} + \frac{k^2}{b^2} + \frac{l^2}{c^2}\right]}$$

or $$d = \frac{1}{\left[\frac{h^2}{a^2} + \frac{k^2}{b^2} + \frac{l^2}{c^2}\right]^{1/2}}$$

For a cubical crystal $a = b = c$

$$\therefore \quad d = \frac{a}{(h^2 + k^2 + l^2)^{1/2}}$$

• 1.16. BRAGG'S LAW

W. L. Bragg discovered that when the X-rays are incident on the crystal surface nearly at glancing angle, they can be regularly reflected by the cleavage planes of the crystals. The cleavage planes are successive atomic planes in the crystal. The intensity of the reflected beam at certain angles will be maximum if two reflected waves from two different planes have a path difference equal to an integral multiple of X-rays wavelength.

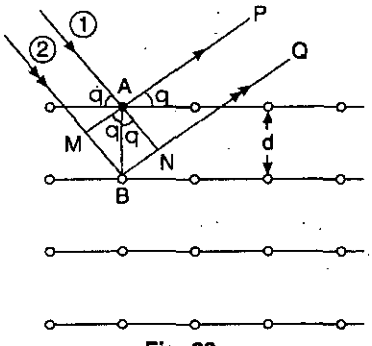


Fig. 29.

Figure 29 shows a particular set of atomic planes in a crystal structure, separated by a distance d. Let an X-ray beam of wavelength λ be incident at a glancing angle θ.

Ray 1, which strikes the upper plane at A, goes towards P after reflection.

Ray 2 strikes the lower plane at point B and goes towards Q after reflection. Draw two perpendiculars AM and AN on incident and reflected ray 2 respectively.

Path differnce between the ray 1 and ray 2 is $MB + BN$.

In triangle AMB, $MB = AB \sin\theta = d \sin\theta$

Hence, path difference $= MB + BN$

$= 2d \sin\theta$

If this path difference is an integral multiple of wavelength λ, constructive interference will take place between the reflected rays. Thus, the intensity will be maximum if

$$2d \sin\theta = n\lambda$$

where $n = 1, 2, 3, \ldots$

This is Bragg's law.

For $n = 1$, we get the Ist order spectrum and for $n = 2$, we get second order spectrum and so on.

• 1.17. DETERMINATION OF CRYSTAL STRUCTURE

With the use of different cleavage planes of the crystal as reflecting surface for the unknown wavelength of X-rays, we determine the lattice constant d and hence find the crystal structure. It is seen that the ratios of lattice constants with one of them as unity depend upon the way in which the atoms are arranged in the crystal.

Let us consider a cubic crystal. The atoms are situated at definite places *i.e.* at each corner of the cube as shown in Figure 30.

The structure is repeated throughout the crystal. It is seen that three sets of planes rich in atoms exist.

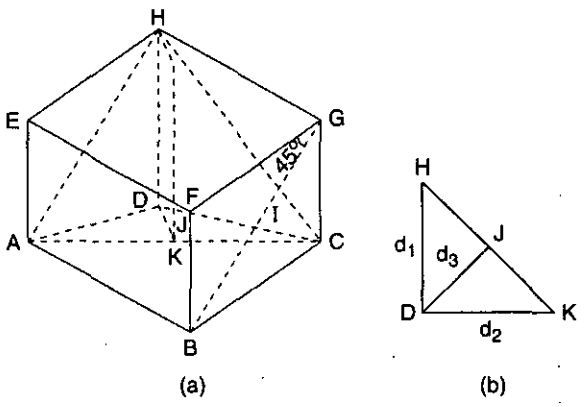


Fig. 30.

(i) The first set of planes such *HEAD*, *BCGF*, *CDHG*, *ABFE*, *EFGH* and *ABCD* are alike. Let the distance between the consecutive planes be d_1. These planes are known as (100) planes.

(ii) The second set of planes consists of parallel planes like *ABGB*, inclined at an angle of 45° to the (100) planes. If d_2 be the interplanar distance for these planes as represented by *FI*, then

$$\frac{d_2}{d_1} = \sin 45° = \frac{1}{\sqrt{2}}$$

$$\therefore \quad d_2 = \frac{d_1}{\sqrt{2}}$$

These planes are (110) planes.

(iii) The third set of planes consists of planes like *ACH*. To find the interplanar distance between these planes, draw *DK* perpendicular to *AC* and join *HK* to complete the right angled triangle *HDK*, shown in Figure 30 (b). From *D* draw *DJ* perpendicular to *HK*. Then, $DJ = d_3$ measures the spacing between these planes. Now in triangle DKH, $DH = d_1, dK = d_2, DJ = d_3$ and $KH = \sqrt{d_1^2 + d_2^2}$.

Also
$$\sin H = \frac{d^2}{KH} = \frac{d_2}{\sqrt{d_1^2 + d_2^2}} = \frac{d_3}{d_1}$$

So,
$$d_3 = \frac{d_1 d_2}{\sqrt{d_1^2 + d_2^2}} = \frac{d_1 \frac{d_1}{\sqrt{2}}}{\sqrt{d_1^2 + \frac{d_1^2}{2}}} = \frac{d_1}{\sqrt{3}}$$

These are (111) planes.

Hence,
$$\frac{1}{d_1} : \frac{1}{d_2} : \frac{1}{d_3} = 1 : \sqrt{2} : \sqrt{3}.$$

Using the KCl crystal, Bragg found the following values of θ for reflection from the faces *EFGH*, *ABGH* and *ACH* respectively. $\theta_1 = 5.22°$, $\theta_2 = 7.30°$, $\theta_3 = 9.05°$.

For the first order spectrum, $\frac{1}{d} = \frac{2 \sin \theta}{\lambda}$

$$\therefore \quad \frac{1}{d_2} : \frac{1}{d_2} : \frac{1}{d_3} = \sin 5.22° : \sin 7.30° : \sin 9.05°$$

$$= 0.0910 : 0.1272 : 0.1570$$

$$= 1 : 1.40 : 1.73$$

Within the limits of experimntal errors, these ratios are $1 : \sqrt{2} : \sqrt{3}$. Hence, we conclude that KCl has a cubic crystal structure.

• 1.18. VERIFICATION OF BRAGG'S LAW FOR NaCl CRYSTAL

NaCl crystals are cubic and every elementary cube has eight ions at its corners, 4 of Na^+ and 4 or Cl^- and form 4 molecules of NaCl. Each ion of NaCl is shared between the two cubes and each elementary cube contains half molecule of NaCl.

$$\text{Mass of elementary cube} = \frac{M}{2N}$$

where M = Molecular weight of NaCl and N = Avogadro's number.

$$\therefore \text{ Mass of elementary cube} = \frac{23 + 35.5}{2 \times 6.02 \times 10^{26}}$$

Volume of elementary cube = d^3

$$\text{Density of NaCl} = 2.17 \times 10^3 \text{ kg/ m}^3$$

So, $$\text{Volume} = d^3 = \frac{58.5}{2 \times 6.02 \times 10^{26} \times 2.17 \times 10^3}$$

or $$d = \left[\frac{58.5}{2 \times 6.02 \times 10^{26} \times 2.17 \times 10^3}\right] = 2.814 \times 10^{-10} \text{ m}$$

According to Bragg's law, $2d \sin\theta = n\lambda$

First order diffraction $n = 1$

$$\therefore \quad \lambda = 2d \sin\theta = 2 \times 2.814 \times 10^{-10} \times \sin 11.8^\circ$$

$$= 5.628 \times 0.2 \times 10^{-10} \text{ m}$$

$$= 1.12 \times 10^{-10} \text{ m} = 1.12 \text{Å}$$

For second order diffraction, $n = 2$

$$\therefore \quad 2\lambda = 2d \sin\theta$$

or $$\lambda = d \sin\theta = 2.814 \times 10^{-10} \times \sin 23.5^\circ$$

$$= 1.12 \times 10^{-10} \text{ m} = 1.12 \text{ Å}$$

For third order diffraction, $n = 3$

$$\therefore \quad 3\lambda = 2d \sin\theta$$

or $$\lambda = \frac{2}{3} d \sin\theta = \frac{2}{3} \times 2.814 \times 10^{-10} \times \sin 36^\circ$$

or $$\lambda = 1.12 \times 10^{-10} \text{ m} = 1.12 \text{Å}$$

Thus, we find that for every order spectrum, $2d \sin\theta = n\lambda$.

Hence, diffraction from NaCl crystal verifies Bragg's law.

• 1.19. LAUE'S METHOD

In Laue's method, a single crystal is held stationary in an *X*-ray beam of continuous wavelength. The crystal selects and produces diffraction corresponding to discrete values of λ for which planes of spacing d exist and incident angle θ satisfies Bragg's law. The experimental arrangement is shown in Figure 31 (a).

Laue's *X*-ray camera consists of a source producing *X*-rays of continuous wavelength (0.2Å to 2 Å), a pin hole collimator for obtaining a fine narrow beam, a single crystal of 1 mm size, a stand which keeps the crystal stationary and two flat films for recording diffraction patterns.

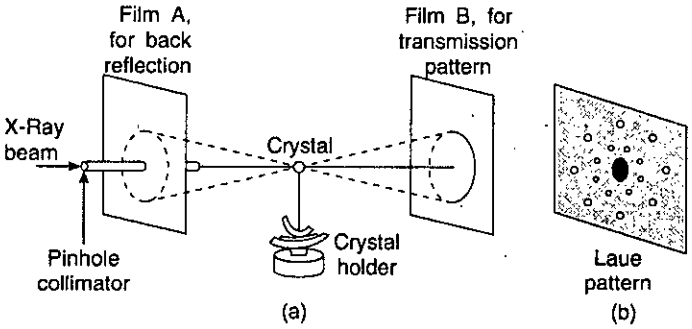


Fig. 31.

Film *B* records the transmission pattern while film *A* records the back reflected pattern. The diffraction pattern consists a series of spots known as Laue spots or Laue pattern which shows the symmetry of the crystal [Figure 31 (b)]. Each spot in this pattern corresponds to an interference, maximum for a set of crystal planes satisfying the Brag's law for a particular wavelength.

The distribution of spots in the pattern depends on the symmetry and orientation of the crystal. This method is convenient for the rapid determination of crystal symmetry and orientation. It is also used for studying the extent of crystalline imperfection under mechanical and thermal treatment.

• 1.20. ROTATING CRYSTAL METHOD

In this method, a single crystal (size upto 1 mm) is rotated about a fixed axis in monochromatic *X*-ray beam. The variation in the angle θ brings different atomic planes of the crystal for reflection. The experimental arrangement is shown in Figure 32. The crystal under investigation is mounted on a rotating spindle; and the film is wrapped on a cylindrical surface co-axial with the spindle. The incident monochromatic *X*-ray beam is diffracted from a given crystal plane when the value of θ satisfies Bragg's relation for the wavelength of *X*-rays used. The beams reflected from all planes parallel to the axis of rotation lie in the horizontal plane while those from planes with other orientation lie below or above the horizontal plane.

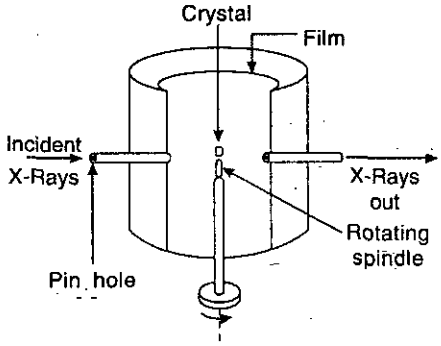


Fig. 32.

The reflected spots form parallel lines. Using Bragg's relation, the spacing *d* can be calculated because λ is known. It may be noted that plane containing incident beam and plane with spacing so small that $\lambda / 2d > 1$ cannot reflect.

This method is the best suited method for structure determination of single crystal. If rotation photographs are taken separately about three axes, the dimensions of the unit cell of the crystal *i.e.* translation vectors $\vec{a}$, $\vec{b}$ and $\vec{c}$ is determined. So this method is a very powerful device for determining the size of a unit cell.

• 1.21. POWDER METHOD

This method of determining the crystal structure was developed independently by Debye and Scherrer in Germany and by Huel in America in 1916. In this method the specimen is a finely powdered polycrystalline solid. The minute crystals of this powder are all randomly oriented so that they make all possible angles with the incident monochromatic *X*-ray beam. Thus all orders of reflection from all possible atomic planes are recorded at the same time. The specimen is contained in a thin walled capillary tube held in a movable mount at the centre of a cylindrical type camera fitted with a photographic film inside as shown in figure 33. Diffracted rays go out from individual crystallites which happens to be oriented so that a particular family of atomic planes in them makes such an angle θ with the incident *X*-ray beam hat the Bragg's relation is satisfied. The diffracted rays leave the specimen along directions which generate a number of cones concentric with the directions of the original beam and make an angle 2θ with it, where θ is the Bragg's angle. The cones intercept the film in a seriesof concentric rings whose arcs are shown in figure 34.

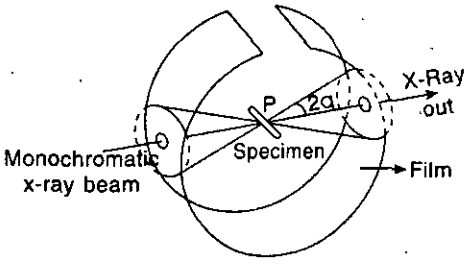


Fig. 33.

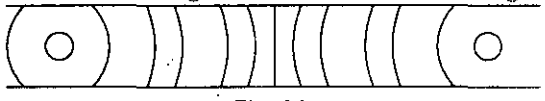


Fig. 34.

These arcs are the intersections of cones with the film. The central spot is due to the direct beam. Different arcs on one side of the central spot correspond to different atomic planes. With the help of these arcs one can find the value of θ. If λ is known, the interplanar distance *d* is obtained. Hence the crystal structure is known.

• TEST YOURSELF

1. What is the difference between crystalline solids and amorphous solids ?

2. What is space lattice ?

3. Explain translation vectors.

4. What is primitive cell ?

• EXERCISE

1. Describe in detail two dimensional lattice types.
2. Describe in detail thre dimensional lattice types.
3. What do you mean by atoms per unit cell ? Calculate its value for simple cubic, face centred cubic and body centred cubic cell.
4. Define coordination number. Calculate its value for s.c., f.c.c. and b.c.c. cells.
5. What do you mean by atomic radius ? Calculate its value for s.c., f.c.c. and b.c.c. lattices.
6. Define atomic packing fraction. Calculate its value for s.c., f.c.c. and b.c.c. lattices.
7. Show that for a cubic lattice, the lattice constant a is given by

$$a = \left(\frac{n M}{Ne}\right)^{1/3}$$

where M is the molecular weight, e is the density of crystal, N is Avogadro's number and n is the number of molecules per unit cell.

8. Describe hexagonal close packed structure (hcp)and calculate its atomic packing fraction.
9. Explain the structure of sodium chloride.
10. Explain the crystal structure of diamond. Calculate its packing fraction.
11. What are Miller indices ? How is the orientation of a plane specified by Miller indices ?
12. Derive the formula for determining the separation between successive lattice planes.
13. Derive Bragg's law of crystal diffraction.
14. Discuss briefly the method to determine the crystal structure.
15. Describe Laue's method for crystal structure analysis.
16. Describe rotating crystal method for X-ray diffraction.
17. Describe powder method for the analysis of crystal structure.
18. The coordination number for an fcc lattice is :

    (a) 2 (b) 6 (c) 8 (d) 12

19. The atomic radius for a simple cubic lattice is :

    (a) $\frac{a}{2\sqrt{2}}$ (b) $\frac{\sqrt{3}\,a}{4}$ (c) $\frac{a}{2}$ (d) a

20. The packing fraction for a bcc lattice is :

    (a) $\frac{\pi}{6}$ (b) $\frac{\sqrt{3}\,.\pi}{8}$ (c) $\frac{\sqrt{3}\,.\pi}{6}$ (d) π

21. The number of constituent particles for an sc lattice is :
(a) 6 (b) 8 (c) 9 (d) 12

22. The number of atoms per unit cell for an fcc lattice is :
(a) 1 (b) 2 (c) 4 (d) 6

23. The number of constituent particles for an fcc lattice is :
(a) 6 (b) 8 (c) 12 (d) 14

24. The density for a bcc lattice is :
(a) $\frac{2A}{Na^3}$ (b) $\frac{A}{Na^3}$ (c) $\frac{A}{2Na^3}$ (d) $\frac{A}{4Na^3}$

25. The nature of lattice of diamond is :
(a) only fcc lattice (b) only bcc lattice
(c) only hcp lattice (d) dual inter lattice structure

26. The number of atoms per unit cell of a bcc lattice is :
(a) 1 (b) 2 (c) 4 (d) 8

27. The atomic radius of bcc lattice is :
(a) $\frac{\sqrt{3}.a}{4}$ (b) $\frac{a}{2\sqrt{2}}$ (c) $\frac{a}{2}$ (d) a

28. The packing factor of a simple cubic lattice is :
(a) $\frac{2A}{Na^3}$ (b) $\frac{A}{Na^3}$ (c) $\frac{A}{2Na^3}$ (d) $\frac{A}{4Na^3}$

29. The number of constituent particles in a bcc lattice is
(a) 8 (b) 9 (c) 12 (d) 16

30. The number of atoms per unit cell for a simple cubic lattice is :
(a) 1 (b) 2 (c) 4 (d) 6

31. The volume of an fcc lattice having N atoms is (a = lattice parameter) :
(a) Na^3 (b) $\frac{Na^3}{2}$ (c) $\frac{Na^3}{4}$ (d) $\frac{Na^3}{8}$

32. The nearest neighbour distance in a simple cubic lattice is :
(a) a (b) $\frac{a}{\sqrt{2}}$ (c) $\frac{a}{\sqrt{3}}$ (d) $\frac{\sqrt{2}.a}{3}$

33. Calcium chloride crystal is :
(a) sc (b) fcc (c) bcc (d) hcp

34. Bragg's law of diffraction is :
(a) $2d \sin\theta = n\lambda$ (b) $2d \cos\theta = n\lambda$
(c) $d \sin\theta = 2n\lambda$ (d) $d \cos\theta = 2n\lambda$

35. Powder method was devised by :
(a) Laue (b) Bragg
(c) Debye and Scherrer (d) None of these

• ANSWERS

18. (d)	**19.** (c)	**20.** (b)	**21.** (b)	**22.** (c)	**23.** (d)
24. (a)	**25.** (d)	**26.** (b)	**27.** (a)	**28.** (b)	**29.** (b)
30. (a)	**31.** (c)	**32.** (a)	**33.** (c)	**34.** (a)	**35.** (c)

U N I T - II

SOLID STATE DEVICES

STRUCTURE

LEARNING OBJECTIVES

After learning this chapter, you will be able to know

- Study of semiconductors
- Study of different diodes namely zener, Tunnel, photodiode, LED, Schottky and Solar cell.
- Half wave and full wave rectifiers.
- Study of bridge rectifiers.
- Study of filtering circuits.
- Study of voltage regulators.

• 2.1. INTRINSIC AND EXTRINSIC SEMI-CONDUCTOR

Intrinsic semi-conductor :

A chemically pure specimen of any semi-conducting material is called intrinsic semi-conductor. For example—pure Germanium or Silicon is an intrinsic semi-conductor.

Extrinsic semi-conductor :

When a very small proportion of an impurity (say few parts per million) is added to a semi-conductor, the electrical conductivity of the resulting material is appreciably increased. The conductivity will depend upon the type and amount of impurity added. **The resulting material *i.e.*, the impure semi-conductor is called extrinsic semi-conductor.** For example — when a small amount of arsenic (pentavalent) or aluminium (trivalent) impurity is added to pure germanium or silicon (tetravalent), the conductivity appreciably increases and the resulting new material is called **extrinsic semi-conductor.**

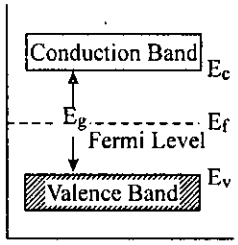


Fig. 1

Density (concentration of electrons in an inrinsic semi-conductor) : Fig. 1 shows the energy band diagram of an intrinsic semi-conductor. At room temperature, some of the electrons in valence band get excited, cross the forbidden gap and enter into the conduction band, leaving behind holes in the valence band. Let us assume that the conduction band has energy equal to E_c and the valence band has energy equal to E_v. If the conduction band is considered to possess infinite number of energy levels, the density of electrons (no. of electrons per unit volume) in the conduction band is given by:

$$n_e = \int_{E_c}^{\infty} Z(E) F(E)\, dE \qquad ...(1)$$

(E_c is the energy at the bottom of the conduction band)

where $Z(E)$ denotes the number of possible energy states per unit volume per unit energy range and $F(E)$ is the Fermi function which gives the probability of an electron occupying a given energy level E. The energy density of states, $Z(E)$ at the bottom of the conduction band of a semi-conductor is given by :

$$Z(E) = \frac{4\pi}{h^3} (2m_e^*)^{3/2} (E - E_c)^{1/2} \qquad ...(2)$$

where m_e^* is the effective mass of the electron in the band. (The concept of effective mass has been taken into account considering the interaction of the neighbouring atoms and charges on the motion of an electron in the band).

The Fermi distribution function is given by

$$F(E) = \frac{1}{e^{(E-E_F)/kT} + 1} \qquad ...(3)$$

Putting the values of $Z(E)$ and $F(E)$ from eqs. (2) and (3) in (1), we get

$$n_e = \int_{E_c}^{\infty} \frac{4\pi}{h^3} (2m_e^*)^{3/2} (E - E_c)^{1/2} \times \frac{1}{e^{(E-E_F)/kT} + 1} dE$$

or

$$n_e = \frac{4\pi}{h^3} (2m_e^*)^{3/2} \int_{E_c}^{\infty} \frac{(E - E_c)^{1/2}}{e^{(E-E_F)/kT} + 1} dE \qquad ...(4)$$

Since the first term in the denominator of the integrand is much greater than unity, so 1 can be neglected. Eqn. (4) can be written as

$$n_e = \frac{4\pi}{h} (2m_e^*)^{3/2} \int_{E_c}^{\infty} (E - E_c)^{1/2}\, e^{(E_F - E)/kT}\, dE$$

$$= \frac{4\pi}{h} (2m_e^*)^{3/2} \int_{E_c}^{\infty} (E - E_c)^{1/2}\, e^{[E_F - E_c + (E_c - E)/kT}\, dE$$

$$= \frac{4\pi}{h} (2m_e^*)^{3/2} \int_{E_c}^{\infty} (E - E_c)^{1/2}\, e^{(E_F - E_c)/kT} \cdot e^{(E_c - E)/kT}\, dE$$

$$= \frac{4\pi}{h} (2m_e^*)^{3/2} \cdot e^{(E_F - E_c)/kT} \int_{E_c}^{\infty} (E - E_c)^{1/2}\, e^{(E_c - E)/kT}\, dE \qquad ...(5)$$

Putting $E - E_c = kTx$ and $dE = kTdx$ in eq. (6), we get (when $x = 0$, $E = E_c$ and when $x = \infty$, $E = \infty$)

$$\therefore \quad n_e = \frac{4\pi}{h^3} (2m_e^*)^{3/2} e^{(E_F - E_c)/kT} \int_{E_c}^{\infty} (kT)^{1/2}\, x^{1/2}\, e^{-x} kT\, dx$$

$$= \frac{4\pi}{h^3}(2m_e^*)^{3/2}(kT)^{3/2}\, e^{(E_F-E_c)/kT} \int_{E_c}^{\infty} x^{1/2}\, e^{-x}\, dx$$

$$= \frac{4\pi}{h^3}(2m_e^*)^{3/2}(kT)^{3/2}\, e^{(E_F-E_c)/kT}\, \frac{\pi^{1/2}}{2} \left[\because \int_0^{\infty} x^{1/2}\, e^{-x}\, dx = \frac{\pi^{1/2}}{2}\right]$$

or
$$\boxed{n_e = 2\left[\frac{2\pi m_e^* kT}{h^2}\right]^{3/2} e^{(E_F-E_c)/kT}} \quad ...(6)$$

Eq. (6) gives the electron concentration (density) in the conduction band of an intrinsic semi-conductor.

[**Note :** The electrons in the conduction band and the holes in the valence band of an intrinsic semi-conductor follow the Fermi-Dirac distribution law.]

Concentration (density) of holes in the valence band : $F(E)$ is the probability for a state of energy E to be occupied by the electron. So the probability for a state of energy E not be occupied by the electron will be $[1 - F(E)]$. Since the hole in the valence band is that state of energy which is unoccupied by the electron, therefore the density of the holes in the valence band is given by replacing $F(E)$ by $[1 - F(E)]$ in eqn. (1).

$$n_h = \int_{-\infty}^{E_v} Z(E)\,[1 - F(E)]\, dE \quad ...(7)$$

where E_v is the energy at the top and $-\infty$ at the bottom of the valence band.

Now
$$1 - F(E) = 1 - \frac{1}{e^{(E-E_F)/kT} + 1} = \frac{e^{(E-E_F)/kT}}{e^{(E-E_F)/kT} + 1}$$

In the valence band $E << E_F$, so $e^{(E-E_F)/kT} << 1$

$\therefore$
$$1 - F(E) = e^{(E-E_F)/kT} \quad ...(8)$$

The value of $Z(E)$ near the top of valence band (most of the holes in the valence band reside near the top) is given by

$$Z(E) = \frac{4\pi}{h^3}(2m_h^*)^{3/2}\,(E_v - E)^{1/2} \quad ...(9)$$

where m_h^* is the effective mass of the hole near the top of the valence band. Therefore, eqn. (7) becomes

$$n_h = \int_{-\infty}^{E_v} \frac{4\pi}{h^3}(2m_h^*)^{3/2}\,(E_v - E)^{1/2} e^{(E-E_F)/kT}\, dE$$

$$= \frac{4\pi}{h^3}(2m_h^*)^{3/2} \int_{-\infty}^{E_v} (E_v - E)^{1/2}\, e^{(E-E_v+E_v-E_F)/kT}\, dE$$

$$= \frac{4\pi}{h^3}(2m_h^*)^{3/2} \int_{-\infty}^{E_v} (E_v - E)^{1/2}\, e^{(E-E_v)/kT}\, e^{(E_v-E_F)/kT}\, dE$$

$$= \frac{4\pi}{h^3}(2m_h^*)^{3/2}\, e^{(E_v-E_F)/kT} \int_{-\infty}^{E_v} (E_v - E)^{1/2}\, e^{(E-E_v)/kT}\, dE \quad ...(10)$$

Putting $E_v - E = kTx$ and $dE = -KT\, dx$ in eqn. (10), we get

[When $x = 0$, $E = E_v$, and when $x = +\infty$, $E = -\infty$]

$$n_h = \frac{4\pi}{h^3}(2m_h^*)^{3/2} e^{(E_v-E_F)/kT} \int_{-\infty}^{E_v} (kT)^{1/2}\, x^{1/2}\, e^{-x}\, (-kT)\, dx$$

$$= \frac{4\pi}{h^3}(2m_h^*)^{3/2} e^{(E_v-E_F)/kT} (kT)^{3/2} \int_{-\infty}^{E_v} x^{1/2} e^{-x}\, dx$$

$$\left[\because \int_{\infty}^{0} f(x)\, dx = -\int_0^{\infty} f(x)\, dx\right]$$

$$= \frac{4\pi}{h^3}(2m_h^*)^{3/2}\,(kT)^{3/2}\, e^{(E_v-E_F)/kT} \cdot \frac{\pi^{1/2}}{2} \qquad \left[\therefore \int_0^{\infty} x^{1/2}\, e^{-x}\, dx = \frac{\sqrt{\pi}}{2}\right]$$

or
$$n_h = 2\left[\frac{2pm_h^* kT}{h^2}\right]^{-3/2} e^{(E_v-E_F)/kT} \quad ...(11)$$

Eqn. (11) gives the hole concentration (density) in the valence band of an intrinsic semi-conductor.

Fermi level in an intrinsic semi-conductor : Since the number of electrons in the conduction band is equal to the number of holes in the valence band of an intrinsic semi-conductor, therefore, the electron density is equal to the hole density *i.e.*

$$n_e = n_h$$

From eqns. (6) and (11)

$$2\left[\frac{2\pi m_e^* kT}{h^2}\right]^{3/2} e^{(E_F - E_c)/kT} = 2\left[\frac{2\pi m_h^* kT}{h^2}\right]^{-3/2} e^{(E_v - E_F)/kT}$$

or $$m_e^{*3/2}\, e^{(E_F - E_c)/kT} = m_h^{*3/2}\, e^{(E_v - E_F)/kT}$$

or $$\frac{e^{(E_F - E_c)/kT}}{e^{(E_v - E_F)/kT}} = \left(\frac{m_h^*}{m_e^*}\right)^{3/2}$$

or $$e^{(E_F - E_c - E_v + E_F)/kT} = \left(\frac{m_h^*}{m_e^*}\right)^{3/2}$$

or $$2E_F - E_c - E_v = \frac{3}{2} kT \log_e \left(\frac{m_h^*}{m_e^*}\right)$$

or $$E_F = \frac{E_c + E_v}{2} + \frac{3}{4} kT \log_e \left(\frac{m_h^*}{m_e^*}\right)$$

This is the expression of Fermi level in an intrinsic semi conductor. When $m_h^* = m_e^*$, $\log_e \left(\frac{m_h^*}{m_e^*}\right) = \log_e (1) = 0$

We get, $$F_F = \frac{E_c + E_v}{2}$$

Thus the Fermi level lies exactly in the middle of the top of valence band and bottom of the conduction band. In fact $m_h^* > m_e^*$ so the Fermi level rises slightly with the rise in temperature T.

• 2.2. LAW OF MASS ACTION FOR INTRINSIC SEMI-CONDUCTOR

The law of mass action for intrinsic semi-conductors state that the *product of electron and hole concentrations for a semi-conductor is constant at a given temperature.*

The electron and hole concentrations in case of intrinsic semi-conductors are given by

$$n_e = 2\left[\frac{2\pi m_e^* kT}{h^2}\right]^{3/2} e^{(E_F - E_c)/kT} \qquad \text{[Eqn. (6)]}$$

i.e., $$n_h = 2\left[\frac{2\pi m_h^* kT}{h^2}\right]^{3/2} e^{(E_v - E_F)/kT} \qquad \text{[Eqn. (11)]}$$

The product

$$n_e n_h = 4\left(\frac{2\pi kT}{h^2}\right)^3 (m_e^* m_h^*)^{3/2}\, e^{(E_F - E_c)/kT}\, e^{(E_v - E_F)/kT}$$

$$= 4\left(\frac{2\pi kT}{h^2}\right)^3 (m_e^* m_h^*)^{3/2}\, e^{(E_v - E_c)/kT}$$

$$= 4\left(\frac{2\pi kT}{h^2}\right)^3 (m_e^* m_h^*)^{3/2}\, e^{-E_g/kT} \qquad \ldots(12)$$

where $E_g = E_c - E_v$ = Band gap energy.

Obviously at a particular temperature T, the product $n_e\, n_h$ is constant and does not depend upon the Fermi level. It depends upon band gap energy E_g. This law holds good for extrinsic semi-conductors also. If the impurity is added, n_e increases and n_h decreases such that the product is constant. In case of intrinsic semi-conductor $n_e = n_h = n_i$ (intrinsic concentration).

$$n_e = n_h = n_i^2 \qquad ...(13)$$

(ii) Temperature dependence of electron and hole concentrations : At 0°K, the semi-conductor behaves as an insulator. It becomes conducting only when the temperature is increased considerably higher than absolute zero. The charge carrier concentration rises with temperature because electrons from lower states of the valence band move to the conduction band. The electron or hole concentration (intrinsic concentration) is given by :

$$n_e = n_h = n_i = 2\left(\frac{2\pi\, kT}{h^2}\right)^{3/2} (m_e^* m_h^*)^{3/4}\, e^{-E_g/2kT} \qquad ...(14)$$

[From eqns. (12) and (13)]

This shows how the concentrations are temperature dependent. Although n_e or n_h n_h is also proportional to $T^{3/2}$ but the variation in the values is mostly dependent on the exponential term $e^{-E_g/2kT}$.

Taking logarithm of both sides of eqn. (14)

$$\log_e n_i = \log_e \text{ constt.} - \frac{E_g}{2kT}$$

If we plot a graph between log n_i and $\frac{1}{T}$, we can study the temperature dependence of intrinsic concentration. The graph is straight line whose slope gives the value of $-\frac{E_g}{2k}$. This provides one of the methods to determine the value of the energy gap E_g of the semiconductor.

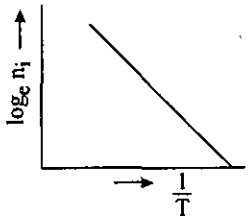


Fig. 2. Plot showing the temperature dependence of intrinsic concentration.

• 2.3. DOPING AND EXTRINSIC SEMI-CONDUCTOR

The intrinsic semiconductor has little current conductivity at room temperature. When a small amount of suitable impurity is added to a pure (intrinsic) semi-conductor, its conducting properties are significantly increased. The semi-conductor is then called **impurity or doped or extrinsic semi-conductor** and the process of adding impurities to a semi-conductor is called **doping.** Generally an extremely small amount (approximately 1 in 10^8 atoms) of impurity is added to the semi-conductor. Depending upon the type of impurity atoms added, the extrinsic semi-conductors are divided into two groups :

(i) n –type semi-conductor

(ii) p –type semi-conductor.

***n*–type semi-conductor** is the semi-conductor in which the number of electrons (negative charge carriers) is much greater than the number of holes produced by thermal agitation.

***p*–type semi-conductor** is the semi-conductor in which the holes (positive charge carriers) are in majority.

Mechanism of conduction in *n*-type semiconductor : When an extremely small, carefully controlled amount of a pentavalent impurity (Arsenic or Antimony) is

introduced into the intrinsic semi-conductor say germanium crystal, the resulting material is known as ***n*-type semi-conductor.**

The addition of pentavalent impurity provides a large number of free electrons in the semi-conductor crystal. When a pentavalent Arsenic (atomic number 33) or Antimony (atomic number 51) is added to germanium or silicon, the impurity atom fits in the germanium crystal in such a way that its four valence electrons form covalent bonds with four germanium atoms. The fifth valence electron of arsenic atom finds no place in covalent bands and therefore, becomes free even at room temperature (shown in Fig. 3). Thus each arsenic atom added, proides one free electron and even an extremely small amount of arsenic impurity provides enough atoms to supply millions of free electrons. Since the impurity atoms donate free electrons to the crystal, the pentavalent impurity is known as **donor.** The crystal is said to be ***n*-type semi-conductor** as the number of electrons (negative charge carriers) is much greater than the number of holes produced due to thermal agitation at the room temperature (*n* stands for negative). Fig. 4 shows the energy band description of *n*-type semi-conductors. In an intrinsic semi-conductor, the allowed energy levels are only either in the valence band or in the conduction band and not in the forbidden band. But due to impurity atoms additional allowed energy levels appear in the forbidden band. The energy of these levels is very small below the conduction band. Its value is only 0.01 eV in germanium and 0.05 eV in Silicon. So at room temperature almost all the donated electrons cross into the conduction band. The recombination of electrons and holes also increases as a result of an increased number of donated electrons and so the number of holes decreases.

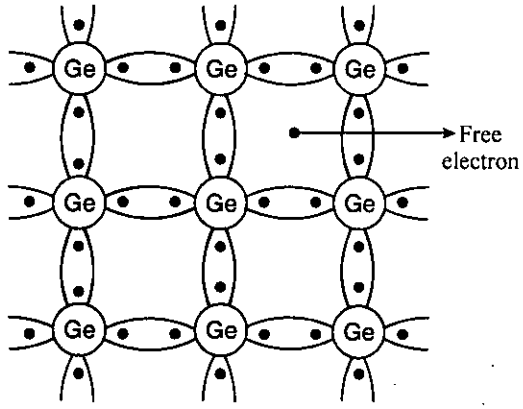
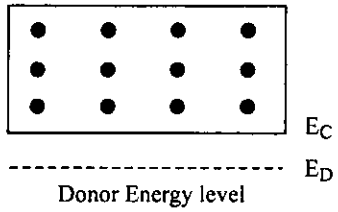


Fig. 3.



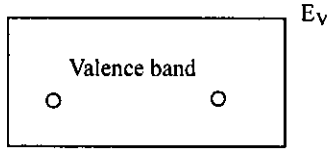


Fig. 4.

When a potential difference is applied across the *n*-type semi-conductor, the donated free electrons are directed towards the positive terminal. The current through the crystal is due to the free electrons (negative charge carriers). So the conductivity is called negative or *n*-type conductivity.

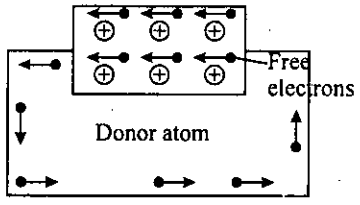


Fig. 5.

Mechanism of conduction in *p*-type semi-conductor : When a small amount of trivalent impurity (gallium, indium or aluminium) is added to an intrinsic semi-conductor, it is called ***p*-type semi-conductor.**

The addition of trivalent impurity provides a large number of holes in the semi-conductor. When a trivalent (indium) is added to germanium, the impurity atom fits in such a way that its three valence electrons form covalent bonds with the three electrons of the neighbouring Ge atoms. The fourth covalent bond has a missing electron, thus a hole is introduced for each impurity atom (figure 6). The hole has a tendency to accept one electron. So the impurity atom is called an **acceptor.** The addition of a very small amount of impurity creates a large number of holes (positive charge carriers) which are mobile. The crystal is said to be ***p*-type semi-conductor** (*p* stands for positive charge).

Figure shows the energy band description of p-type semi-conductors. The impurity introduces an allowable discrete energy level (0.01 eV) just above the valence band. This helps the electrons to leave the valence band and occupy the acceptor level as the energy required is very small. Thus a large number of holes (charge carriers) are generated in the valence band. Therefore, in p-type semi-conductor the electrons are the minority and holes are the majority charge carriers. When a potential difference is applied across the p-type semi-conductor, the holes being positively charged, are directed towards the negative terminal, causing hole current. The conductivity is called positive or p-type conductivity.

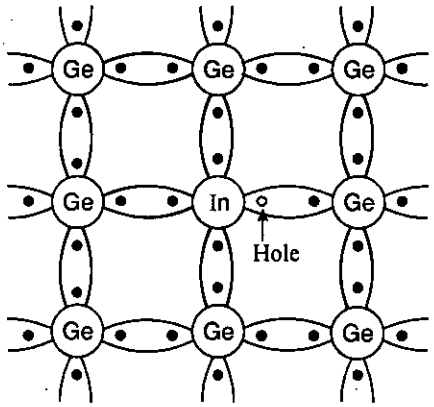


Fig. 6.

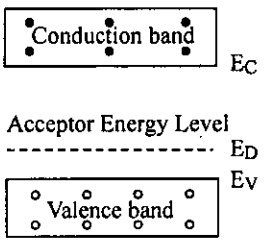


Fig. 7.

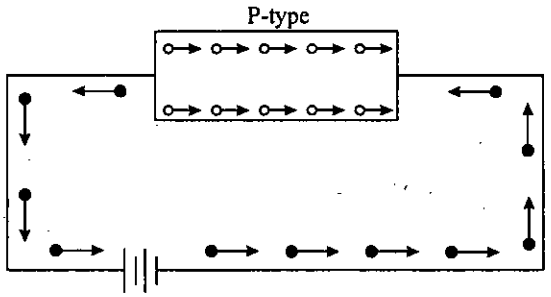


Fig. 8.

• 2.4. CONCENTRATION (DENSITY) OF ELECTRONS IN AN n-TYPE SEMI-CONDUCTOR

In impurity semi-conductor, the impurity atoms reduce the energy gap. In n-type semi-conductor the donor level is just below the lower edge of the conduction band as shown in the Fig. (9). Let E_d denotes the energy of the donor level and N_d the number of donor atoms per unit volume. The density of electron in the conduction band is given by

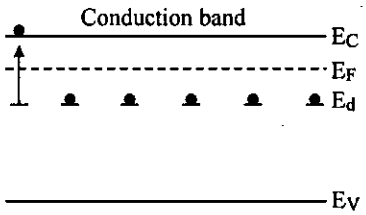


Fig. 9.

$$n_e = 2\left[\frac{2\pi m_e^* kT}{h^2}\right]^{3/2} e^{(E_F - E_c)/kT} \qquad ...(15)$$

So the number of vacancies per unit volume in the donor level (Density of empty donors) is

$$N_d\,[1 - F(E)] = N_d\left[1 - \frac{1}{e^{(E_d - E_F)/kT} + 1}\right]$$

[where $F(E)$ is the probability for a state of energy E to be occupied by the electron.]

$$= N_d\left[\frac{e^{(E_d - E_F)/kT}}{1 + e^{(E_d - E_F)/kT}}\right]$$

$$= \frac{N_d}{1 + e^{(E_F - E_d)/kT}} \qquad ...(16)$$

Since the concentration of electrons in the conduction band is equal to the number of vacancies per unit volume in the donor level, so from equations (15) and (16)

$$2\left[\frac{2\pi m_e^* kT}{h^2}\right]^{3/2} e^{(E_F - E_c)/kT} = \frac{N_d}{1 + e^{(E_F - E_d)/kT}} \qquad ...(17)$$

It can be assumed that E_F lies more than few kT above the donor level and so 1 can be neglected from the denominator of R.H.S. of eqn. (17)

$$\therefore \quad 2\left[\frac{2\pi m_e^* kT}{h^2}\right]^{3/2} e^{(E_F - E_c)/kT} = N_d\,[e^{(F_d - E_F)/kT}] \quad ...(18)$$

Taking logarithm, we get

$$\log_e 2\left[\frac{2\pi m_e^* kT}{h^2}\right]^{3/2} + \frac{E_F - E_c}{kT} = \log_e N_d + \frac{E_d - E_F}{kT}$$

or $$\frac{E_F - E_c}{kT} - \frac{E_d - E_F}{kT} = \log_e N_d - \log_e 2\left[\frac{2\pi m_e^* kT}{h^2}\right]^{3/2}$$

Putting the value of E_F in eqn. (15), we get

or $$\frac{2E_F - E_d - E_c}{kt} = \log_e\left[\frac{N_d}{2\left(\frac{2\pi m_e^* kT}{h^2}\right)^{3/2}}\right]$$

or $$E_F = \frac{E_d + E_c}{2} + \frac{kT}{2} = \log_e\left[\frac{N_d}{2\left(\frac{2\pi m_e^* kT}{h^2}\right)^{3/2}}\right] \quad ...(19)$$

$$n_e = 2\left[\frac{2\pi\, m_e^* kT}{h^2}\right]^{3/2} \cdot e^{\frac{\left[\frac{E_d + E_c}{2} + kT\log_e\left[\frac{N_d}{2(2\pi m_e^* kT/h^2)^{3/2}}\right] - E_c\right]}{kT}}$$

$$= 2\left[\frac{2\pi\, m_e^* kT}{h^2}\right]^{3/2} e^{\frac{E_d - E_c}{2kT} + \frac{1}{2}\log_e\left[\frac{N_d}{2\,(2\pi\, m_e^* kT/h^2)^{3/2}}\right]}$$

$$= 2\left[\frac{2\pi m_e^* kT}{h^2}\right]^{3/2}\left[e^{\frac{E_d - E_c}{2kT}\log_e\left\{\frac{N_d}{2(2\pi m_e^* kT/2)^{3/2}}\right\}^{3/2}}\right]$$

$$= 2\left[\frac{2\pi m_e^* kT}{h^2}\right]^{3/2} \cdot \left(\frac{N_d}{2}\right)^{1/2} \frac{1}{\left(\frac{2\pi\, m_e^* kT}{h^2}\right)^{3/4}} e^{(E_d - E_c)/2kT}$$

$$= (2n_d)^{1/2}\left\{\frac{2\pi m_e^* kT}{h^2}\right\}^{3/4} e^{(E_d - E_c)/kT}$$

or $$n_e = (2N_d)^{1/2}\left(\frac{2\pi m_e^* kT}{h^2}\right)^{3/4} e^{-\Delta E/2kT} \quad ...(20)$$

where $\Delta E = E_c - E_d$ is called **ionisation energy** of donors.

Eqn. (20) gives the density of electrons in the conduction band of an *n*-type semi-conductor. Obviously, the density of electrons in the conduction band is directly proportional to the square root of the donor concentration.

Effect of temperature on the position of Fermi level and electron density : At absolute zero ($T = 0°K$) the eqn. (19) reduces to

$$E_F = \frac{E_d + E_c}{2}$$

This shows that the Fermi level lies exactly half way between the donor levels and the bottom of conduction band. The donor levels are all occupied but there are no electrons in the conduction band. As the temperature is increased the Fermi level falls below the donor level as the electrons are raised from donor levels to the conduction band and at high temperature E_F approaches the centre of forbidden gap (bottom of the conduction band and top of the valence band $\left(E_F \simeq \frac{E_c + E_v}{2}\right)$. This is due to the

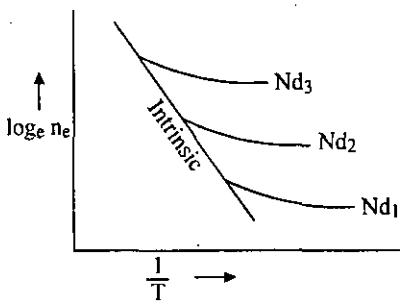


Fig. 10.

thermal excitation of electrons from the valence band to the conduction band. At this stage the semi-conductor becomes intrinsic. Figure (10) shows the variation of electron concentration with temperature. The graph is plotted between $\log_e n_c$ and $\frac{1}{T}$ for the extrinsic semi-conductor with different donor densities $(N_{d_1} < N_{d_2} < N_{d_3})$.

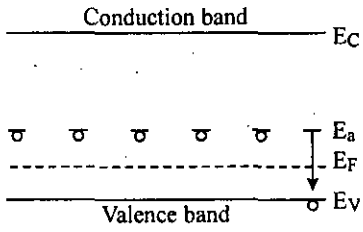


Fig. 11.

Concentration (density) or holes in a *p*-type semi-conductor : The Fig. (11) shows the energy level diagram of *p*-type semi-conductor. The acceptor level is just above the top of the valence band. Let N_a denotes the number of acceptor atoms per unit volume and E_a the energy of the acceptor level. The density of the holes in the valence band is given by

$$n_h = 2\left[\frac{2\pi m_h^* kT}{h^2}\right]^{3/2} e^{(E_v - E_F)/kT} \quad ...(21)$$

[See equation (11)]

The number of electrons per unit volume in the acceptor level is

$$= N_a F(E) = \frac{N_a}{e^{(E_a - E_F)/kT} + 1}$$

Since, $E_a - E_F >> kT$, so 1 can be neglected from the denominator.

$\therefore$ density of electrons in the acceptor level is

$$= N_a e^{(E_F - E_a)/kT} \quad ...(22)$$

The number of electrons in the acceptor level is equal to the number of holes in the valence band. Therefore, from eqns. (21) and (22),

$$2\left[\frac{2\pi m_h^* kT}{h^2}\right]^{3/2} e^{(E_v - E_F)/kT} = N_a e^{(E_F - E_a)/kT} \quad ...(23)$$

Taking lorarithm, we get

$$\log_e 2\left[\frac{2\pi m_h^* kT}{h^2}\right]^{3/2} + \frac{E_v - E_F}{kT} = \log_e N_a + \frac{E_F - E_a}{kT}$$

or $$\frac{E_F - E_a}{kT} - \frac{E_v - E_F}{kT} = -\log_e N_a + \log_e 2\left[\frac{2\pi m_h^* kT}{h^2}\right]^{3/2}$$

or $$\frac{2E_F - (E_a + E_v)}{kT} = -\log_e \frac{N_a}{2\left[\frac{2\pi m_h^* kT}{h^2}\right]^{3/2}}$$

$$\text{or} \quad E_F = \frac{E_a + E_v}{2} - \frac{kT}{2} \log \frac{N_a}{2\left[\frac{2\pi m_h^* kT}{h^2}\right]^{3/2}} \quad \ldots(24)$$

Putting the value of E_F in (21), we get

$$n_h = 2\left[\frac{2\pi m_h^* kT}{h^2}\right]^{3/2} e^{\frac{\left[E_v - \frac{E_a+E_v}{2} + \frac{kT}{2}\log\frac{N_a}{2(2\pi m_h^* kT/h^2)^{3/2}}\right]}{kT}}$$

$$= 2\left[\frac{2\pi m_h^* kT}{h^2}\right]^{3/2} e^{\frac{E_v - E_a}{2kT}} . e^{\frac{1}{2}\log_e \frac{N_a}{2(2\pi m_h^* kT/h^2)^{3/2}}}$$

$$\text{or} \quad n_h = 2\left[\frac{2\pi m_h^* kT}{h^2}\right]^{3/2} e^{\frac{E_v - E_a}{2kT}} \left(\frac{N_a}{2}\right)^{1/2} \times \frac{1}{\left(\frac{2\pi m_h^* kT}{h^2}\right)^{3/4}}$$

$$= (2N_a)^{1/2}\left[\frac{2\pi m_h^* kT}{h^2}\right]^{3/4} e^{\frac{E_v - E_a}{2kT}}$$

$$\text{or} \quad n_h = (2N_a)^{1/2}\left[\frac{2\pi m_h^* kT}{h^2}\right]^{3/4} e^{-\frac{\Delta E}{2kT}} \quad \ldots(25)$$

where $\Delta E = E_a - E_v$.

The eqn. (25) gives the density of holes in the valence band of a *p*-type semi-conductor. It is obvious that the density of the holes in the valence band is proportional to the square root of the acceptor concentration.

Effect of temperature on the position of Fermi level : At absolute zero ($T = 0°K$) the eqn. (24) reduces the

$$E_F = \frac{E_a + E_v}{2}$$

The Fermi level lies exactly hal way between the acceptor level and the top of the valence band. As the temperature increases, the Fermi lvel rises above th acceptor level and at high temperature E_F approaches the centre of forbidden gap and the semi-conductor becomes intrinsic. This is due to the fact that at low temperatures, the conduction is due mostly to the impurity. At high temperatures there is thermal excitation of valence electrons.

• 2.5. DIFFUSION AND DRIFT

Charge carries move through semi-conductor materials by two separate mechanisms.

(i) Diffusion : When there is a concentration of free charge carriers (of the same kind) in one part of the crystal, the mutual repulsion between the charge carriers results in a net movement of charges from an area of high concentration to one of low concentration. This is known as **diffusion.**

(ii) Drift : When an electric field is applied to a semi-conductor, the electron move towards the positive end and the hole (empty space caused by the movement of electron) towards the negative end of the semi conductor constituting the drift current. Thus Drift is an effect resulting from the application of an electric field to the semi-conductor. In *p*-type semi-conductor the drift current is caused by the movement of holes whereas in *n*-type semi-conductor the drift current is due to the motion of electrons.

Drift velocity and mobility : When a potential difference is applied across a crystal, the charge carriers attain a drift velocity which is directly proportional to the applied electric field intensity. If E be the electric field and v_d the drift velocity, then

$$v_d \propto E \qquad \text{or } v_d = \mu E$$

where μ is called **mobility** of the charge carriers. Thus the **mobility** of charge carrier is defined as its **drift velocity produced by unit field intensity.**

Conductivity of semi-conductor : If n_e be the density of electrons in the conduction band of semi-conductor the total charge per unit volume of the band is $n_e e$. If the drift velocity of an electron due to electric field E is v_{de}, the current density j is given by

$$j = n_e e v_{de} \qquad ...(26)$$

We know that $v_{de} = \mu_e E$

$$\therefore \qquad j = n_e e \mu_e E \qquad ...(27)$$

where μ_e is the mobility of electron.

But $$j = \sigma_e E \qquad ...(28)$$

where σ_e in the conductivity of the semi-conductor due to the electrons in the conduction band. From eqns. (27) and (28), we have

$$\sigma_e = n_e e \mu_e \qquad ...(29)$$

Similarly if n_h denotes the density of holes in the valence band of semi-conductor, its conductivity due to holes is given by

$$\sigma_h = n_h e \mu_h \qquad ...(30)$$

where μ_h is the mobility of hole.

The total conductivity of semi-conductor σ due to electrons in the conduction band and holes in the valence band is given by

$$\sigma = \sigma_e + \sigma_h$$

Using eqns. (29) and (30)

$$\sigma = n_e e \mu_e + n_h e \mu_h = e (n_e \mu_e + n_h \mu_h) \qquad ...(31)$$

(i) Electrical conductivity of intrinsic semi-conductor : For intrinsic semi-conductor, the density of electrons in the conduction band n_e is equal to the density of holes in the valence band n_h. So

$$n_e = n_h = n_i$$

where n_i is the number of charge carriers (electrons or holes) per unit volume of the intrinsic semi-conductor. In this case, the equation (31) takes the form

$$\sigma = e n_i (\mu_e + \mu_h) \qquad ...(32)$$

We know that $$n_i = 2\left(\frac{2\pi kT}{h^2}\right)^{3/2} (m_e^* m_h^*)^{3/4} e^{-E_g/2kT}$$ [See eqn. (14)]

Putting the value of n_i in eqn. (32), we have

$$\sigma = 2e (\mu_e + \mu_h)\left(\frac{2\pi kT}{h^2}\right)^{3/2} (m_e^* m_h^*)^{3/4} e^{-E_g/2kT} \qquad ...(33)$$

The conductivity depends upon temperature as depicted in the above equation.

(ii) Electrical conductivity of extrinsic semi-conductor : The extrinsic semi-conductors are of two types :

(i) n-type (ii) p-type

***n*-type semi-conductor :** The electrical conductivity is mainly due to electrons in the conduction band. So for n-type semi-conductor, the electrical conductivity is given by

$$\sigma = n_e \mu_e e$$

We know that

$$n_e = \frac{N_d}{1 + e^{(E_F - E_d)/kT}}$$

$$\therefore \quad \sigma = \frac{e\mu_e N_d}{1 + e^{(E_F - E_d)/kT}} \qquad ...(34)$$

p-type semi-conductor : The electrical conductivity is due to the holes in the valence band and so can be written as

$$\sigma = n_h \; e\,\mu_h$$

We know that $$n_h = \frac{N_a}{1 + e^{(E_a - E_F)/kT}}$$

$$\therefore \quad \sigma = \frac{e\,\mu_h \; N_a}{1 + e^{(E_a - E_k)/kT}}$$

• 2.6. *p-n* JUNCTION DIODE

The *p-n* junction diode or semi-conductor diode is an electron device which has a high resistance to the flow of current in one direction and a low resistance in the opposite direction. The semi-conductor diodes consist of *p-n* junctions formed in silicon or germanium crystals.

***p-n* junction and diode :** When a *p*-type semi-conductor is suitably joined to *n*-type semi-conductor, the contact surface is called ***p-n* junction.** The *p-n* junction is of great importance. The semi-conductor containing *p-n* junction is called **semi-conductor diode.** To obtain a *p-n* junction diode, the semi-conductor (silicon or germanium) is doped with donor atoms at one end and acceptor atoms at the other. This semi-conductor crystal has both *p*-type and *n*-type regions which create a junction between them. The *p*-type and *n* type portions of the diode are called anode and cathode respectively in reference to the vacuum tube. The direction in which the diode resistance is small is shown by the arrow head.

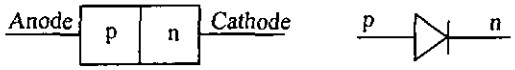


Fig. 12.

Potential barrier in a *p-n* junction : The Fig. (13) shows the *p-n* junction. Initially holes majority carriers are present to the left of the junction and electron majority carriers to the right of the junction. There are a few minority charge carriers on each side. A density gradient is set up across the junction resulting in diffusion of holes to the right and electrons to the left of the junction. As the electrons leave the *n*-type material, donor ions are produced on the *n*-side of the junction. When these electrons fill holes on the *p*-side of the junction, the acceptor ions are produced. Thus there is a net negative charge at the *p*-side and net positive charge on the *n*-side of the junction as shown in the Fig. 13. The space occupied between these ions is called the **space charge region** or **depletion region.** It is called so because the mobile charge carriers *i.e.* free electrons and holes have been depleted (emptied) is this region. Across this region, a potential difference is developed and thus an internal electric field E_i is produced which stops further diffusion of majority charge carriers. The potential difference across the depletion region is of the order of 0.1 to 0.3 volts and is called the **potential barrier.** Outside this barrier on each side of the junction, the material is neutral.

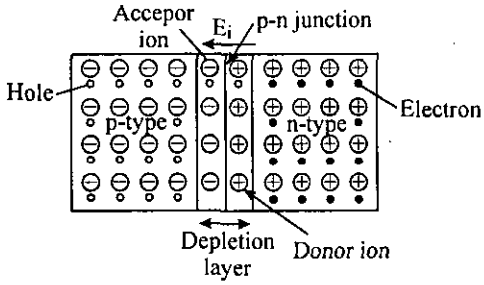


Fig. 13.

The change distribution, the internal electric field and the potential barrier in the depletion region are shown as in the Fig. (14).

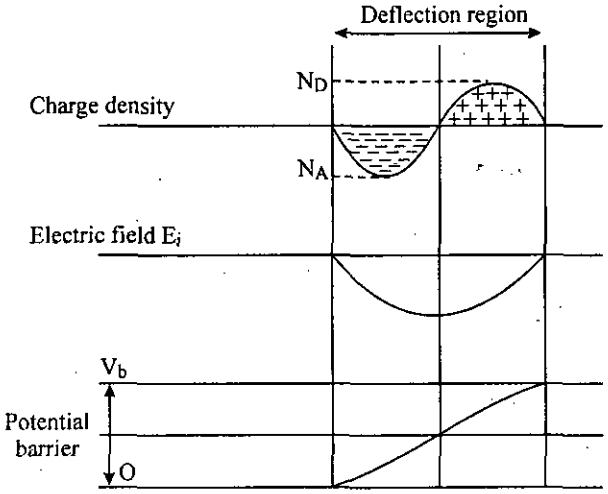


Fig. 14.

• 2.7. BEHAVIOUR OF *p-n* JUNCTION

When an external battery is connected across the *p-n* junction diode, it is called biasing. In the absence of biasing or when the external voltage is zero, the potential barrier at the junction does not permit current flow. Therefore, the circuit current is zero. There are two methods of biasing a diode :

(a) Forward biasing and (b) Reverse biasing.

(a) Forward biasing of a diode : When a battery is connected across a *p-n* junction in such a way that its positive terminal is connected to the *p*-side and the negative terminal to the *n*-side, the diode is said to be **forward biased** as shown in the Fig. 15. Under the influence of of forward voltage, the free electrons in *n*-region and the holes in the *p*-region move towards the junction. The drift of holes and electrons towards the junction reduces the width of the depletion region and also the potential barrier. The free electrons crossing the junction combine with the holes in the *p*-region. The positive and the negative terminals of the battery are considered to supply holes and electrons to the *p*-side and the *n*-side of the diode respectively. The diffusion of majority charge carriers constitute a current across the junction and the total current is the sum of the hole and the electron currents. The resultant current in the *p*-region is a hole current and in the *n*-region, is electron current. However, in the connecting wires, the current is carried by electrons.

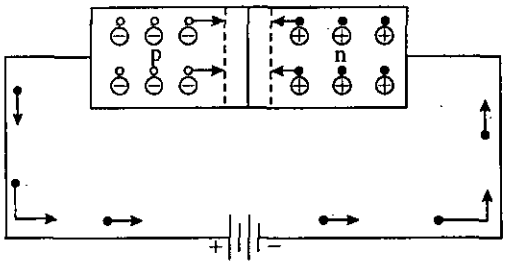


Fig. 15.

Volt -Ampere characteristics under forward biasing : V-I characteristic of a semi-conductor diode (*p-n* junction)is the curve showing the variation of circuit current with the vltage applied across the junction. This can be studied by the circuit arrangement shown in the Fig. 16. When the forward voltage is increased from zero, the potential barrier is reduced, more majority charge carriers cross the junction and the forward current flows across the junction. In the beginning the current increases very slowly (shown by the portion *OA* of the curve Fig. 17). When the forward voltage becomes more than the junction potential, the barrier disappears and the current increases rapidly but it is limited by the circuit resistance (shown by the linear

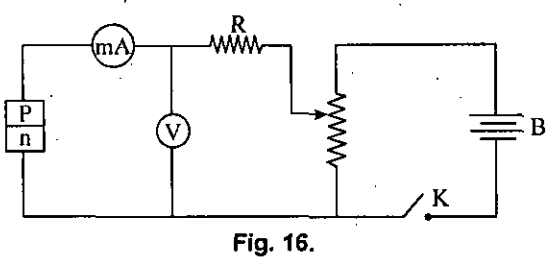


Fig. 16.

portion AB of the characteristic curve). The p-n junction offers very small resistance in the forward biasing. The forward current is due to the majority carriers produced by the impurity.

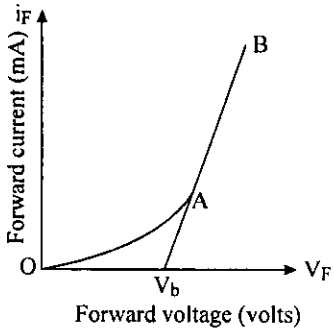


Fig. 17.

(b) Reverse biasing of a diode : When the positive terminal of the battery is connected to the n-type and the negative terminal to the p-type of a p-n junction diode, it is said to be **reverse biased** as shown in the Fig. (18). Under the effect of reverse voltage, the holes and the electrons of the p-region and n-region respectively are drifted away from the junction. This increases the width of the depletion region and also the potential barrier. Therefore the junction resistance becomes very high and a very small current (μ A) flows from the n-region to the p-region. This is called **reverse current** and is due to the minority charge carriers as the applied reverse bias appears as forward bias to them. When the reverse bias is increased, more majority charge carriers are unable to cross the potential barrier, thereby decreasing the majority charge carrier current. Hence the net current from the n-region to the p-region increases until a point is reached when no majority charge carrier is able to cross the barrier. The constant current at this stage is equal to the minority charge current called **reverse saturation current.** If the reverse bias is further increased, a critical voltage called **breakdown voltage** is reached, when a rapid increase in current takes place as shown in the Fig. (19). The reverse current is due to the minority carriers due to breaking of some covalent bonds at room temperature.

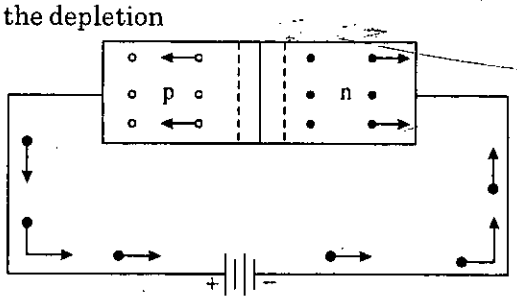


Fig. 18.

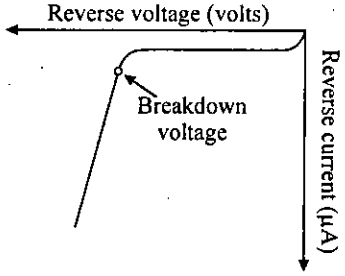


Fig. 19.

• 2.8. KNEE VOLTAGE

Under the effect of forward biasing of the p-n junction diode, the current rises very slowly until the potential barrier is overcome. Then it starts increasing rapidly. ***The forward voltage at which the current through the junction starts to increase rapidly is called knee voltage.*** The knee voltage for silicon diode is 0.7 V and for germanium diode it is 0.3 V. In order to get useful current through a p-n junction, the applied voltage must be more than the knee voltage.

(b) Breakdown voltage : Under the effect of reverse biasing of the p-n junction, a very small current flows through the junction even at the room temperature. Some minority carriers are produced in the depletion layer. When the junction is reverse biased, the electrons move towards the positive terminal of the battery. At high reverse voltage, these electrons acquire energies high enough to liberate valence electrons from semi-conductor atoms. The electrons thus liberated, in turn free other valence electrons. Thus a very large reverse current is obtained. At this stage the junction may breakdown. ***This, reverse volage at which p-n junction breaks down with sudden rise in reverse current is called breakdown voltage.*** The reverse voltage across a p-n junction must always be less than the breakdown voltage.

(c) Zener breakdown and avalanche breakdown : In 1934, C. Zener suggested that under the influence of very intense electric fields (several million volts/cm), electrons can tunnel through the forbidden energy gap. This is true in semi-conductor p-n junction diodes with thin depletion layer, when breakdown occurs with anode voltages in the region of –2.6 V to –5V. This type of breakdown is known as **zener**

breakdown. With wider depletion layers, breakdown occurs at much higher voltage. In such cases the breakdown is due to **avalanche breakdown.**

The mechanism of breakdown can be explained as follows :

Leakage current in *p-n* junctin diode is largely due to the drift of minority carriers across the junction under the influence of the reverse bias. If the electric field in the region of the junction is sufficiently great, the electrons are accelerated and acquire energy high enough to ionise atoms by collision and generate electron-hole pairs in the depletion layer.

Thus, when the reverse voltage applied across a *p-n* junction becomes high enough to impart sufficient energy to the minority charge carriers, some of the covalent bonds are broken due to their collision with the semi-conductor atoms. The large number of electrons and holes thus produced is responsible for the rapid rise in the saturation current. This phenomenon is known as **avalanche breakdown** or **zener breakdown.**

(d) Peak inverse voltage (PIV) : At high reverse voltage applied to a *p-n* junctin, a very large reverse current is obtained, which may destroy the junction due to excessive heat. ***The maximum reverse voltage that can be applied to the p-n junction without damaging the junction is called peak inverse voltage (PIV).***

(e) Maximum forward current : It is defined as ***the maximum instantaneous forward current that can be conducted through the p-n junction without damaging it.*** If the forward current exceeds this value, the junction may be destroyed due to overheating.

(f) Maximum power rating : There is a limit to the voltage that can be applied and the current that can be conducted though the junction without damaging it. Therefore, the maximum power is also limited. ***The maximum power dissipated at the junction is equal to the product of junction current and the voltage across the junction.*** This is a very important factor and must be kept in consideration while using a $p-n$ junction diode.

• 2.9. FERMI LEVELS UNDER ZERO BIASING

In the *p*-type semi-conductor the Fermi energy level is close to the top of the valence band while in *n*-type semi-conductor, it is close to the bottom of the conduction band. When a $p-n$ junction is formed, holes flow from the *p*-region into the *n*-region and electrons flow from the *n*-region to the *p*-region *i.e.* in the opposite direction. An equilibrium is reached when the Fermi levels in the two regions are along the same line as shown in the Fig. 20 (a). Even after the equilibrium stage, the two currents neutralise each other and the net current is zero.

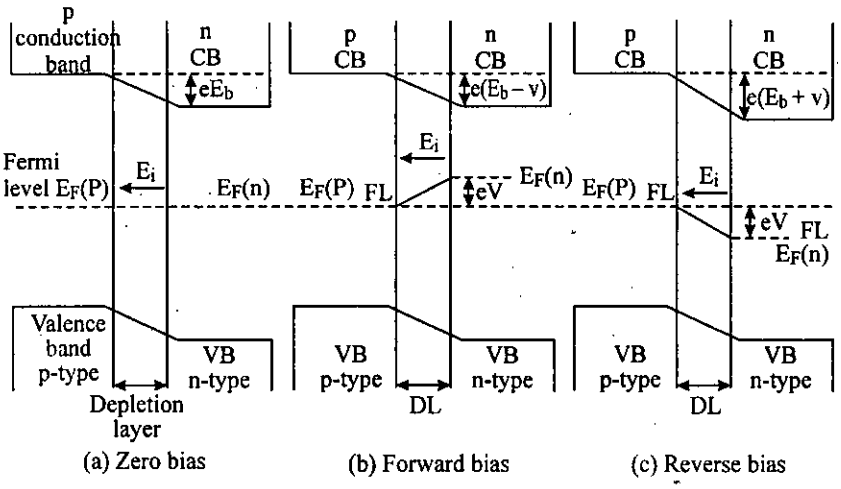


Fig. 20.

Fermi levels under forward biasing : In the forward biasing, the positive terminal of the supply battery is connected to the p-side the negative terminal to the n-side of the $p-n$ junction diode. The energy of the electrons in n-type region increases by an amount eV where V is the applied voltage. The Fermi level rises by eV as shown in Fig. 20 (b). The potential barrier is reduced by $e\,(E_b - V)$.

Fermi levels under reverse biasing : In the reverse biasing the positive terminal of the supply battery is connected to the n-side and negative terminal to the p-side of the $p-n$ junction diode. The energy of the electrons in n-type region decreases by an amount eV. The Fermi level lowers by an amount eV shown in the Fig. 20 (c). The potential barrier now increases to $e\,(E_b + \upsilon)$.

• 2.10. ZENER DIODE

When a semi conductor diode is reverse biased and the reverse voltage is increased, the breakdown voltage is reached when the reverse current increases sharply. This breakdown was first explained by scientist C. Zener. The breakdown voltage and the current are also called Zener voltage and Zener current respectively. The zener voltage depends upon the amount of doping. When an ordinary semi-conductor diode is heavily and properly doped, it has a sharp breakdown voltage and such a device is called 'Zener diode'. Fig. 21 (a) shows the symbol and Fig. 21 (b) shows the reverse characteristic of a zener diode. V_z is Zener potential.

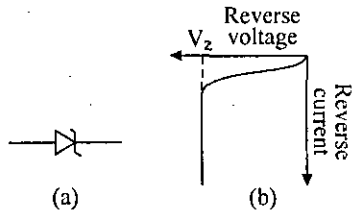


Fig. 21.

Working : Under the effect of reverse biasing, the current remains almost constant over a wide voltage range upto a limit when the current increases sharply due to a sudden increase in he number of electron-hole pairs. This limit of the reverse voltage can be adjusted by varying the doping levels as the zener potential V_z decreases by increasing the doping. If the diode is heavily doped, depletion layer becomes thin and consequently the breakdown voltage will be lower. The Fig. 22 (a) shows the energy level diagram of an unbiased heavily doped diode. The Fermi level in the p-region is closer to the valence band and in the n-region, it is closer to the conduction band. However, the two line up. When the reverse voltage is applied, the energy levels in the n-region moves down relative to those in the p-region. At the zener voltage V_z, the bottom of the conduction band in the p-region get lower than the top of the valence band in the p-region as shown in figure 22 (b). The electrons now directly cross the potential barrier from the valence band in the p-region into the conduction band in n-region.

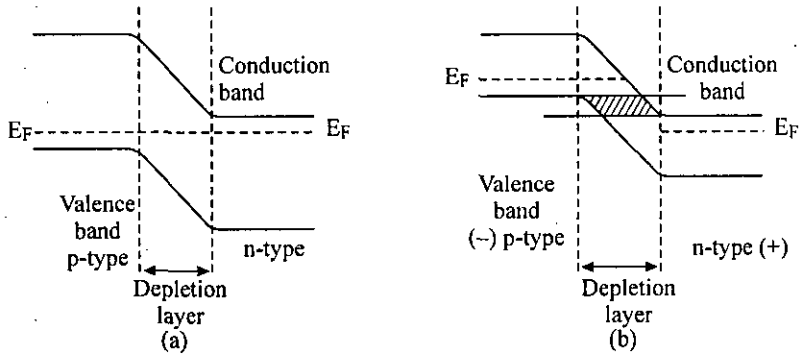


Fig. 22. (a) Unbiased heavily doped p-n junction diode, (b) Reverse biased heavily doped p-n junction diode.

Use of zener diode as voltage stabilizer : A zener diode can be used as voltage stabilizer to provide a constant voltage from a source whose voltage varies over a wide range. The circuit arrangement is shown in the Fig. 23. The zener diode of

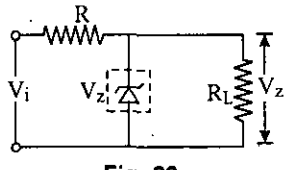


Fig. 23.

zener voltage V_z is reverse biased. It is connected in parallel to a load R_L across which constant voltage is required. R is a series resistance to absorb the output voltage fluctuations.

The zener voltage/current characteristic shows that in the breakdown region, a small change in voltage produces a large variation in the current. If there is a small change in the supply voltage, the current in the circuit increases. But since large changes in the diode current produces very small change in zener voltage, the voltage across the load remains almost unchanged. The excess voltage is dropped across the series resistance R.

• 2.11. TUNNEL DIODE

As discussed in case of zener diode, when the p-n junction is heavily doped, the depletion layer becomes very thin, the electrons can now penetrate through the junction barrier and pass from one side of the layer to the other with less energy than is ordinarily required. This phenomenon is called ***tunneling effect*** and ***the p-n junction diode based upon the quantum mechanical phenomenon of potential barrier penetration is known as tunnel diode.***

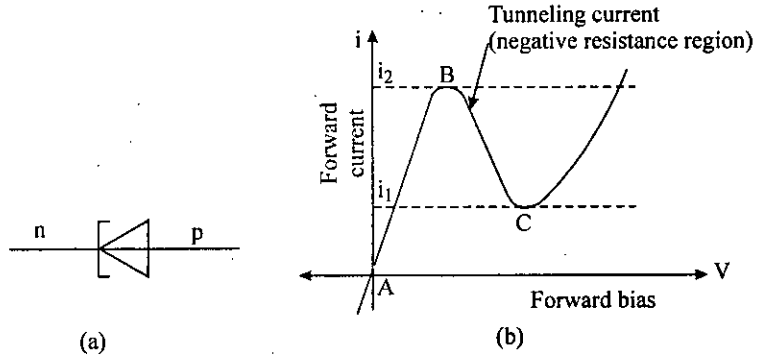


Fig. 24. (a) Shows the symbol (b) Shows the voltage-current characteristics of a tunnel diode.

Working : When the p-n junction diode is heavily doped (impurity concentration 10^{-3} whereas in ordinary diode it is 10^{-8}), the width of the depletion layer is reduced to less than 100° A and the potential barrier becomes very small. Thus the probability of an electron to penetrate the barrier becomes very large. The voltage-current characteristic is now completely different as shown in the Fig. 24 (b). There is a negative resistance region from B to C and that is why a tunnel diode is also called a negative resistance device.

The energy level diagram of a tunnel diode is as shown in the Fig. 25. In case of unbiased tunnel diode, the deplection region is very small ($\simeq 10^{-8}$) and the donor and acceptor levels, merge into the bottom of the conduction band of n-region and into the top the valence band of p-region respectively. The electrons can cross (tunnel) directly through the barrier.

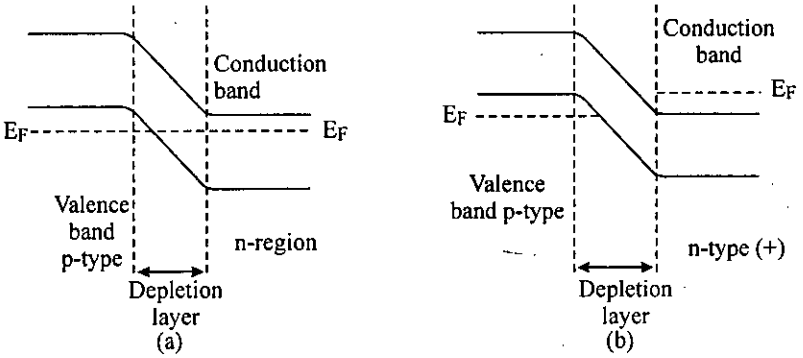


Fig. 25. (a) Unbiased tunnel p-n junction diode, (b) Forward biased tunnel p-n junction diode.

When the junction diode is forward biased the energy levels in the n-type move up relative to those in the p-type and the number of electrons tunneling from the n-region to the p-region increases resulting in the flow of current which first increases and then decreases with increase in forward bias voltage as shown in the voltage current characteristic (Part AB and BC). The decreases in current is due to the fact that the number of empty states in the p-region valence band available for the n-region conduction band electrons now decreases *i.e.* tunneling of electrons is reduced when the forward voltage is further increased, the current rises again due to the diffusion of majority charge carriers across the junction (Part CD of the characteristic curve).

Uses : From the characteristic curve shown in the Fig. 24, it is evident that for currents between i_1 and i_2, the voltage is triple valued that is the same current can be obtained for three different values of applied voltage. This multivalued feature of the tunnel diode makes it specially useful in the high speed switching circuits. Tunnel diodes can also be used as oscillators of very high frequencies. The equivalent circuit of a tunnel diode in negative resistance ($-R_n$) region is shown in the Fig. 26.

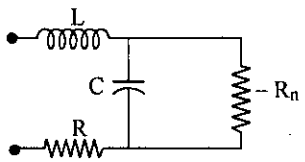


Fig. 26.

• 2.12. LIGHT EMITTING DIODE

Under the effect of forward biasing of a $p-n$ junction diode, majority charge carriers cross the junction and during the movement holes and electrons recombine near the junction thereby releasing some energy. The energy thus released may be in the form of heat or light radiations. In case of germanium and silicon semi-conductor, the energy released is in the form of light radiations. The p-n junction diodes based upon the phenomenon of **electro-luminiscence** are known as **Light emitting diodes (LED).** One form of gallium arsenide LED in sectional view is shown in the Fig. 27. It consists of an n-type layer of gallium arsenide phosphide which is grown upon a gallium arsenide substrate. A very thin p-region is diffused into the n-type layer and an anode in the shape of a comb is laid down in the p-region. The shape of the anode is so as to minimise its masking effect on the emitted light. These diodes are used in display devices, digital read-out devices, pilot lamps and tuning indicators etc.

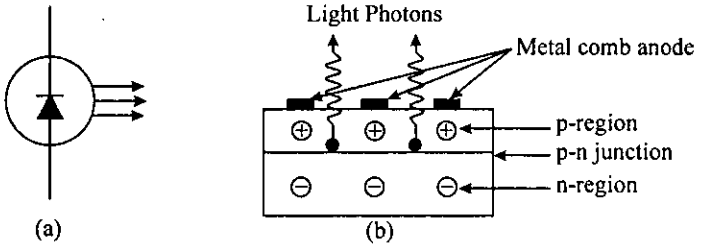


Fig. 27. (a) Symbol of LED, (b) Sectional view of a LED.

• 2.13. PHOTODIODE

The photo-diode is a p-n junction semiconductor diode based upon the phenomenon of the photo voltaic effect. When light radiations are made to fall upon a reverse biased p-n junction diode, a voltage is generated across the junction, due to which a current starts flowing in the circuit. This current varies almost linearly with the incident light intensity.

Working principle : When a p-n junction is reverse biased and in the absence of incident light, a very small almost constant reverse current flows through the circuit. This is due to minority charge carriers (E_0 characteristic curve shwon in the Fig. 28 (b). When light radiations are made to fall on the p-n junction, more hole-electron pairs are formed, their number depends upon the

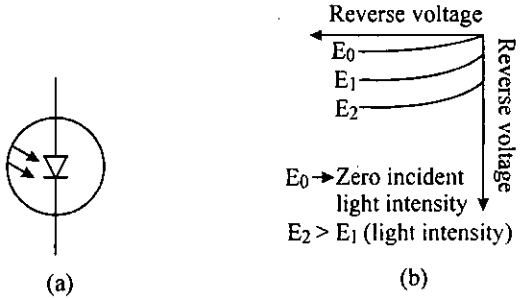


Fig. 28. Photodiode (a) Symbol, (b) Characteristic curve (voltage-current).

intensity of incident light. The electrons thus excited in the conduction band of the p-region diffuse through the junction to the n-region and the holes produced in the valence band of the n-region diffuse through the junction to the p-region and thus add to the current which varies linearly with the incident light intensity. If the incident light falls at a distance from the junction, the minority carriers produced due to the incident light may recombine before diffusing through the junction and a small current will flow. This photo-current increases if the light is incident near the junction. Thus the photo-current is a function of incident light intensity as well as the distance from the junction at which the light is incident.

Uses : Photodiodes are extensively used in industry, photography and light intensity measurements. These are used in high speed computers, light detection systems, light operated switches and counting of objects etc.

• 2.14. SCHOTTKY DIODE

A Schottky diode is a rectifying metal to semi-conductor junction diode. The working of this diode is based upon the property of solids that when a strong electric field is applied to the solids that when a strong electric field is applied to the solids, electrons are emitted which have energies normally possessed by the electrons which leave a hot body. That is why the **Schottky diode** is also known as **hot carrier diode.** Several metals *e.g.*, gold, molybdenum, titanium, chromium etc. are used with either n-type or p-type silicon as a semi-conductor since it possesses better high frequency performanc.

There is a difference between the current flow in the Schottky diode and that in usual p-n junction diode. The minority carriers (holes in the n-type semi-conductors) do not take any part in the current conduction process. This has the effect of achieving switching speeds less than 0.1 ns, resulting in the use of Schottky diodes at very high frequencies upto about 40 GHz.

• 2.15. SOLAR CELL

A solar cell or a photo voltaic cell is a p-n junction semi-conductor device which generates an emf between its terminals when light radiations fall upon it.

Construction : It is made in the form of a silicon p-n crystal. One of the regions (n-type shown in Fig. 29) is a very thin layer (about 1 μm thick) through which light passes without much loss of energy. Top contact of the cell is in the form of comb like structure and the bottom contact covers the entire area. There is an anti-reflection coating at the top so that most of the incident light is absorbed. Fig. 29 (a) shows the symbol and (b) shows the sectional view of the silicon solar cell.

Principle of working : When the light is incident on the top surface of the cell, and reaches the p-n junction, its energy is released into the crystal lattice. This generates electrons and holes in the junction and the diffusion of charge carriers take place. Since one of the regions is very thin, it gets rapidly saturated with the charge carriers, a potential difference developes between the two regions, resulting in flow of current in the external circuit. Thus the p-n junction, under the effect of light radiations act as a cell.

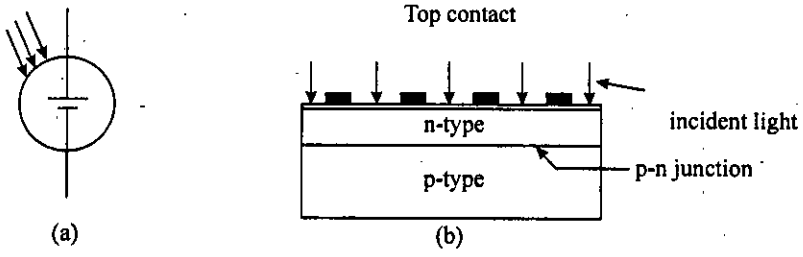


Fig. 29. (a) Symbol (b) Solar cell.

Uses : Solar cells are used in exposure meters, punched tape and card readers and aerospace projects. The use of solar cells as energy source is comparatively expensive.

So these are specially used in space vehicles where the small mass of the solar batteries is of importance.

• 2.16. RESISTANCE OF A CRYSTAL DIODE

We know that a forward biased crystal diode conducts easily whereas a reverse biased diode conducts very small current. We can say that the forward resistance of a diode is very small and the reverse resistance is very high. An ideal diode must offer zero resistance in forward biasing and infinitely large resistance in the reverse biasing.

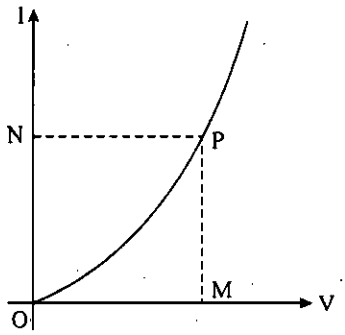


Fig. 30. Forward V- I characteristic.

Forward resistance : When the diode is forward biased, the resistance offered by it is called the **forward resistance.** This resistance is different for the direct current and the changing current. So the resistance is of two types (a) d.c. forward resistance and (b) a.c. or dynamic forward resistance.

(a) d.c. forward resistance : It is the resistance offered by the diode to the direct current and is equal to the ratio of d.c. voltage across the diode to the resulting direct current through it.

$$\text{d.c. forward resistance} = \frac{\text{d. c. voltage across diode}}{\text{resulting direct current}}$$

The Fig. 30 shows the forward V-I characteristic of a crystal diode. We see that when *OM* is the direct voltage applied to the diode, *ON* is the resulting direct current.

$$\therefore \quad \text{d.c. forward rsistance } R_{dc} = \frac{OM}{ON}$$

(b) a. c. forward resistance : It is the resistance offered by the crystal diode to the changing forward current and is equal to the ratio of change in voltage across the diode to the change in the resulting current through it *i.e.,* a.c. forward resistance,

$$R_{a.c.} = \frac{\text{change in voltage across diode}}{\text{resulting change in current through diode}}$$

If *P* be the operating point on V-I characteristic shown in the figure 31. *DF* is the resulting change in current corresponding to the change in voltage A. C., then the a. c. forward resistance is given by

$$R_{a.c.} = \frac{AC}{DF}$$

Reverse resistance : When the crystal diode is reversed biased, the resistance offered by it is called the **reverse resistance.** This resistance is also of two types (a) d.c. reverse resistance and (b) a.c. reverse resistance. These resistances can also be determined in the same way from the V-I characteristics under reverse biasing of the diode as in case of forward biasing.

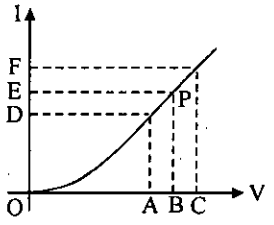


Fig. 31. Forward V- I characteristic.

The reverse resistance of an ideal diode is infinite. However, in practice, the reverse resistance is not infinite. It is very large compared to the forward resistance. In germanium diodes, the ratio of the reverse to the forward resistance is nearly 40000 : 1 whil in silicon diodes the ratio is 1000000 : 1.

• 2.17. CAPACITANCE OF A *p-n* JUNCTION DIODE

A *p-n* junction junction diode has a capacitive effect and therefore, it may behave as a circuit element. There are two types of capacitive effects (a) **diffusion capacitance,** (b) **transition capacitance.** Though both types of capacitance are present in the forward and reverse bias regions, but only one is prominent in each region. In forward bias region we have the diffusion capacitance while in case of reverse bias region, we have the transition capacitance.

Diffusion or storage capacitance : This capacitive effect occurs nder forward biased conditions. The potential barrier is reduced under the effect of forward biasing. The holes from *p*-region enter *n*-region and electrons from *n*-region enter *p*-region. These charge carriers diffuse away from the junction and recombine. The density of the carriers is high near the junction and decreases exponentially with distance. Thus in the forward biasing, the charge is stored on both sides of the junction and varies with the applied potential. This feature is true for a capacitor. This capacitance of the *p-n* junction is called **diffusion** or **storage capacitance** and can be defined as $(C_d = dq / dV)$ the ratio of the change in the charge stored outside the depletion region to the change in potential supplied across the junction. The storage capacitance may have a value of several hundred picofarads.

Transition or Depletion Capacitance : The width of the depletion layer is a function of the junction voltage when the *p-n* junction is reverse biased, the depletion layer widens with the reverse voltage. As the depletion layer is free from charge carriers, it behaves as an insulator or dielectric. The *p*-region and *n*-region behave like good conductors. Thus a *p-n* junction behaves as a parallel plate capacitor. The capacitance is called **transition** or depletion capacitance which decreases with increase in the applied **reverse voltage.** This can be shown that the capacitance varies inversely as the cube root of the applied voltage. The capacitance usually has a value ranging from 5 pico farads to 20 pico farads. The junction diodes which are operated under reverse biased conditions to give variable reactance effect are known as **varactor diodes.**

• 2.18. STATIC AND DYNAMIC CHARACTERISTICS OF A *p-n* JUNCTION DIODE

A **characteristic curve** is a graph drawn between the voltage applied across the *p-n* junction diode and the current obtained in the circuit. When the d.c.voltage is applied, the curve between the voltage and current is called **static characteristic curve** and when the a. c. voltage is applied, the curve is known as **dynamic characteristic curve.**

Static characteristic curve and load line : The Fig. 32 (a) shows a basic diode circuit which consists of a *p-n* junction diode *D* in forward bias in series with a load resistance R_L and a battery of e.m.f. *E*. Fig. 32 (b) shows the static characteristic curve obtained from the diode circuit by having *different values of* V_D and the corresponding values of current *I*. The e.m.f. equation of the circuit is

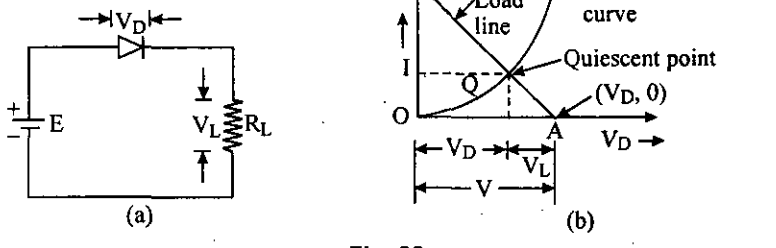


Fig. 32.

$$E = V_D + V_L = V_D + I.R_L \qquad ...(i)$$

From this equation when *I* is zero, $E = V_D$. We get point $A\,(V_D\,,\,0)$ on the voltage axis and when $V_D = 0$, we get the point $B\left(0, \frac{E}{R_L}\right)$ on the current axis. The line *AB* which satisfies eqn. (i) is called **load line.** The point *Q* obtained by the intersection of the load line with the static characteristic curve is called **quiescent point** or **operating point.** The load line given by eqn. (i) can also be expressed as

$$I = \frac{E}{R_L} - \frac{V_D}{R_L} = -\frac{1}{R_L} V_D + \frac{E}{R_L} \qquad ...(ii)$$

Comparing eq. (ii) with the standard eqn. of a straight line $y = mx = c$, we find that slope $m = -\frac{1}{R_L}$ and the intercept $c = \frac{E}{R_L}$. Thus the slope of the load line gives the value of $\left(-\frac{1}{R_L}\right)$ *i.e.,* higher is the value of the load resistance, lesser is the negative slope of the load line.

Dynamic characteristic curve : The Fig. 33 (a) shows the basic *p-n* junction diode circuit which consists of a junction diode D in forward bias in series with a load resistance R_L and an a. c. source S. The Fig. 33 (b) shows the characteristic curve for the diode. For an interval of instantaneous voltage V_i different load lines are drawn. Obviously the load lines are parallel. These lines intersect the static characteristic at the points A and B. We draw horizontal lines A and B and vertical lines from V_i' and V_i which intersect at A' and B. Similarly other points are determined. The curve passing through A', B etc. is known as **Dynamic characteristic curve.** For different value of the load resistance, a different dynamic characteristic is obtained.

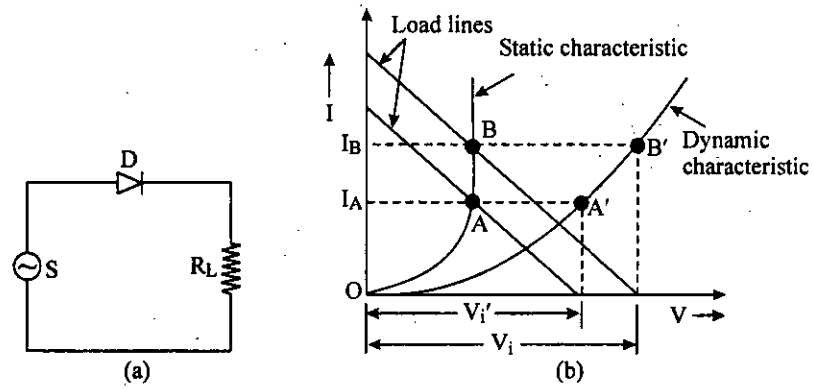


Fig. 33.

• 2.19. RECTIFIER

The process of converting a. c. voltage into d.c. voltage is called **rectification** and the circuit or the apparatus used for this conversion is known as **rectifier.** The following two rectifier circuits can be used (a) Half wave rectifier (b) Full wave rectifier.

***p-n* junction diode as a half wave rectifier :** The *p-n* junction diode is well suited for this purpose as it conducts large current in the forward biasing and a very small current in the reverse biasing. In half wave rectification, the rectifier conducts current during the positive half cycle of the input a. c. supply and no current during the negative half cycle. Therefore, the current flows in one direction through the load. Fig. 34 (i) shows the circuit for the diode half wave rectifier. The a. c. supply to be rectifid is connected in series with the diode and the load resistance through a transformer. The use of transformer gives two advantages. Firstly, the input a. c. voltage can be stepped up or down and secondly the transformer isolates the rectifier circuit from the power supply reducing the risk of electric shock. Fig. 34 (ii) shows the a.c. input and the rectified output voltage.

Working : The a. c. source is connected across the primary MN of the transformer. The polarity of the source change, after every half cycle. The same change takes place in the secondary PQ also. During the positive half cycle of the input, the *p-n* junction is

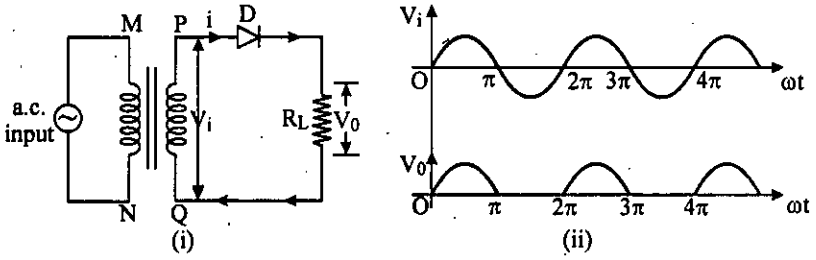


Fig. 34.

forward biased and there is flow of current in the load and during the negative half cycle of the input, the junction is reverse biased and practically there is no flow of current in the load. Thus, the current in the load is in one direction only *i.e.* the output is d. c., though it is pulsating in nature as shown in the Fig. 34 (ii). The output is smoothened by the help of filter circuits. The output of the half wave rectifier is low, as the power is delivered during the half period only.

(a) Efficiency of half wave rectifier : The *efficiency of a rectifier is defined as the ratio of the d.c. power output to the input a.c. power.*

$$\text{Efficiency } \eta = \frac{\text{d.c. power output}}{\text{input a.c. power}}$$

d.c. power output : If i_{dc} be the average d.c. output current during the positive half cycle and R_L be the load resistance, the d.c. power output is

$$P_{dc} = i_{dc}^2 R_L \qquad ...(i)$$

This can be shown that the average d.c. is

$$i_{dc} = \frac{i_0}{\pi} = \frac{1}{\pi}\left[\frac{E_0}{R_D + R_L}\right] \qquad ...(ii)$$

where R_D is the dynamic resistance of the diode and E_0 is the peak value of the a.c. input voltage.

$$\left[i_{dc} = \frac{1}{T}\int_0^{T/2} i_{dt} = \frac{1}{T}\int_0^{T/2} i_0 \sin \omega t \, dt = \frac{\omega}{2\pi}\int_0^{\pi/\omega} i_0 \sin \omega t \, dt = \frac{i_0}{\pi}\right]$$

The d.c. power output is from (i)

$$P_{dc} = \left(\frac{i_0}{\pi}\right)^2 R_L = \left(\frac{1}{\pi}\cdot\frac{E_0}{R_D + R_L}\right)^2 R_L \qquad ...(iii)$$

a.c. power input : It i_{rms} be the average input current, the a.c. power input is given by

$$P_{ac} = i_{\text{rms}}^2 (R_D + R_L) \qquad ...(iv)$$

This can be shown that the average a.c. is

$$r_{\text{rms}} = \frac{i_0}{2} = \frac{E_0}{2(R_D + R_L)} \qquad ...(iv)$$

$$\left[i_{\text{rms}}^2 = \frac{1}{T}\int_0^{T/2} i^2 dt = \frac{\omega}{2\pi}\int_0^{\pi/\omega} i_0^2 \sin^2 \omega t \, dt = \frac{i_0^2}{4}\right]$$

The a.c. power input is from (iv),

$$P_{ac} = \frac{i_0^2}{4}(R_D + R_L)$$

$$= \frac{E_0^2}{4(R_D + R_L)^2}(R_D + R_L)$$

$$= \frac{E_0^2}{4(R_D + R_L)}$$

Putting the vlaues of P_{dc} and P_{ac}, we have the efficiency

$$\eta = \frac{P_{dc}}{P_{ac}} = \frac{\dfrac{i_0^2 R_L}{\pi^2}}{\dfrac{i_0^2}{4}(R_D + R_L)}$$

$$= \frac{4}{\pi^2}\left[\frac{R_L}{R_D + R_L}\right]$$

$$= \frac{4}{\pi^2}\left[\frac{1}{1+(R_D / R_L}\right]$$

or $$\eta = 0.406\left[\frac{1}{1+(R_D / R_L)}\right]$$

The efficiency depends upon the ratio $\left(\frac{R_D}{R_L}\right)$. The lower is the ratio, higher is the efficiency of a rectifier. The efficiency is maximum, if the ratio $\frac{R_D}{R_L} = 0$. Therefore the maximum efficiency of the half wave rectifier is 0.406 or 40.6%. That is a maximum of 40.6% of the a.c. input power is converted into output d.c. power in case of half wave rectifier.

(b) Ripple factor : The output of a rectifier consists of a d.c. component and an a.c. component. The a.c. component is also known as ripple which is undesirable in the output. So smaller is the ripple, greater is the effectiveness of the rectifier. **Ripple factor** of rectifier is ***defined as the ratio of the r.m.s. value of a.c. component to the d.c. component in the rectifier output.***

$$\text{Ripple factor } r = \frac{\text{r.m.s. value of a.c. component}}{\text{value of d.c. component}}$$

$$= \frac{i_{ac}}{i_{dc}}$$

By definition, the r.m.s. value of the total load current is given by

$$i_{\text{rms}} = \sqrt{i_{dc}^2 + i_{ac}^2}$$

or $$i_{ac} = \sqrt{i_{\text{rms}}^2 - i_{dc}^2}$$

Dividing by i_{dc}, we get

$$\frac{i_{ac}}{i_{dc}} = \frac{\sqrt{(i_{\text{rms}}^2 - i_{dc}^2)}}{i_{dc}} = \sqrt{\frac{i_{\text{rms}}^2}{i_{dc}^2} - 1}$$

Putting the values of i_{rms} and i_{dc}, we get

$$\text{Ripple factor } r = \frac{i_{ac}}{i_{dc}}$$

$$= \sqrt{\frac{(i_0 / 2)^2}{(i_0 / \pi)^2} - 1}$$

$$= \sqrt{\frac{\pi^2}{4} - 1} = 1.21$$

Since the ripple factor is greater than unity, the a.c. component which is undesired is more than the d.c. component. Hence the half wave rectifier is not useful for the purpose of rectification.

• 2.20. JUNCTION DIODE AS A FULL WAVE RECTIFIER

A full wave rectifier rectifies both the positive and negative half cycles of the a.c. input. That is the output current is d.c. for both the half cycles of the applied input. This is possible if two *p-n* junction diodes are used. For positive half cycle of the input, one diode supplies current to the load and for the negative half cycle, the other diode supplies the current in the load is always in the same direction. The Fig. 35 (i) shows the circuit for the *p-n* junction full wave rectifier. The circuit consists of two *p-n* junction diodes D_1 and D_2 connected with the secondary of a transformer whose primary is

connected with the a.c. input to be rectified. The secondary PQ is centrally tapped with the load resistance R_L. The Fig. 35 (ii) shows the a.c. input and the full wave rectified output.

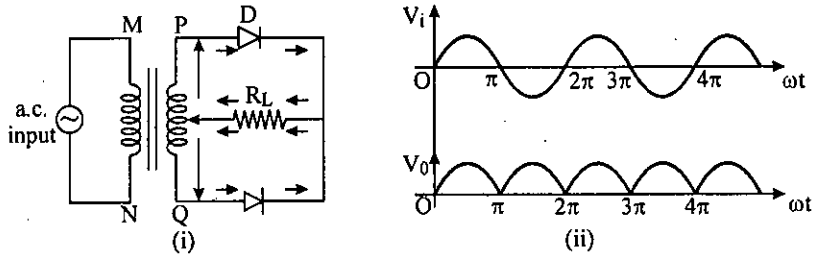


Fig. 35.

Working : During the positive half cycle of the secondary voltage, the P of the secondary becomes positive and the other end Q becomes negative. The junction diode D_1 becomes forward biased and conducts current through the load while the junction diode D_2 becomes reverse biased and practically does not conduct any current. During the negative half cycle of the secondary voltage, the end P becomes negative and Q becomes positive. This makes the junction D_1 reverse biased and D_2 forward biased. Now the current flows through the load from D_2 only in the same direction as shown in the Fig. 35 (i). Thus the output current is unidirectional full wave but pulsating in nature as shown in Fig. 30 (ii).

Efficiency of a full wave rectifier : The efficiency of a rectifier is defined as the ratio of d.c. output power to the a.c. input power.

$$\eta = \frac{P_{dc}}{P_{ac}} \qquad ...(i)$$

The **d.c. value of output current** i_{dc} can be shown equal to $\frac{2i_0}{\pi}$

$$\left[i_{dc} = \frac{1}{T}\left\{ \int_0^{T/2} i_0 \sin \omega t \, dt - \int_{T/2}^{T} i_0 \sin \omega t \, dt \right.\right.$$

$$= \frac{\omega}{2\pi} \int_0^{\pi/\omega} i_0 \sin \omega t \, dt - \int_{\pi/\omega}^{2\pi/\omega} i_0 \sin \omega t \, dt$$

$$= \frac{2i_0}{\pi} = \frac{2E_0}{\pi(R_D + R_L)}$$

The output current is obtained during both the positive and negative half cycles. R_D is the dynamic resistance of each junction diode and R_L is the load resistance.

The d.c. output power

$$P_{dc} = i_{dc}^2 R_L = \frac{4i_0^2}{\pi^2} . R_L \qquad ...(ii)$$

The **r.m.s. value of the output current** i_{rms} can be shown equal to

$$\frac{i_0}{\sqrt{2}} = \frac{E_0}{\sqrt{2}(R_D + R_L)}$$

$$\left[i_{rms}^2 = \frac{1}{T}\left[\int_0^T i^2 dt = \frac{\omega}{2\pi} i_0^2 \sin^2 \omega t = \frac{i_0^2}{2} \right.\right.$$

$$\therefore \quad i_{rms} = \frac{i_0}{\sqrt{2}} = \left.\left. \frac{E_0}{\sqrt{2}(R_D + R_L)} \right]\right]$$

The a.c. input power

$$P_{ac} = i_{rms}^2 (R_D + R_L) = \frac{i_0^2}{2}(R_D + R_L) \qquad ...(iii)$$

$$\eta = \frac{P_{dc}}{P_{ac}}$$

$$= \frac{\frac{4i_0^2}{\pi^2} R_L}{\frac{i_0^2}{2}(R_D + R_L)}$$

$$= \frac{8}{\pi^2}\left(\frac{R_L}{R_D + R_L}\right)$$

or $$\eta = \frac{0.812}{1 + \frac{R_D}{R_L}}$$

The efficiency of the rectifier depends upon the ratio $\frac{R_D}{R_L}$. Lower is this ratio, higher is the efficiency of a rectifier. If the ratio $\frac{R_D}{R_L} = 0$, the efficiency will be maximum equal to 0.812 or 81.2%. The maximum efficiency of a half wave rectifier is 40.6%. Thus the maximum efficiency of a full wave rectifier is twice than that of a half wave rectifier.

Ripple factor of a full wave rectifier : The ripple factor r is given by

$$r = \frac{i_{ac}}{i_{dc}} = \frac{\sqrt{i_{\text{rms}}^2 - i_{dc}^2}}{i_{dc}}$$

or $$r = \sqrt{\left(\frac{i_{\text{rms}}}{i_{dc}}\right)^2 - 1}$$

For full wave rectifier $i_{\text{rms}} = \frac{i_0}{\sqrt{2}}$ and $i_{dc} = \frac{2i_0}{\pi}$

$$\therefore \quad r = \sqrt{\left(\frac{i_0/\sqrt{2}}{2i_0/\pi}\right)^2 - 1}$$

$$= \sqrt{\left(\frac{\pi}{2\sqrt{2}}\right)^2 - 1}$$

$$= \sqrt{\frac{\pi^2}{8} - 1}$$

$$= 0.482$$

The ripple factor for a full wave rectifier is 0.482 which is much less than that for a half wave rectifier ($r = 1.21$). Higher value of efficiency and lesser value of ripple factor make a full wave rectifier very suitable for the purpose of rectification.

• 2.21. FULL WAVE BRIDGE RECTIFIER

The *p-n* junction full wave rectifier is known as centre-tap full wave rectifier, as the secondary winding of the transformer is centre-tapped. This rectifier has the following disadvantages :

(i) It is difficult to locate the position of the centre-tapping on the secondary windings of the transformer.

(ii) The centre-tapping divides the voltage across the secondary windings and so each diode utilises only half of the voltage. Hence the d.c. output is small.

(iii) The peak inverse voltage of the diodes used must be high.

To overcome the above shortcomings, a full wave bridge rectifier is used where the need of centre tapping is eliminated.

Full wave bridge rectifier : It consists of four diodes D_1, D_2, D_3 and D_4 connected so as to form a bridge *ABCD* as shown in the Fig. 36. The a.c. supply to be rectified is connected with the primary windings *MN* of the transformer. The secondary windings *PQ* is connected to the diagonally opposite ends *B* and *D* of the bridge. Load resistance R_L is connected between the other two ends *A* and *C* of the bridge.

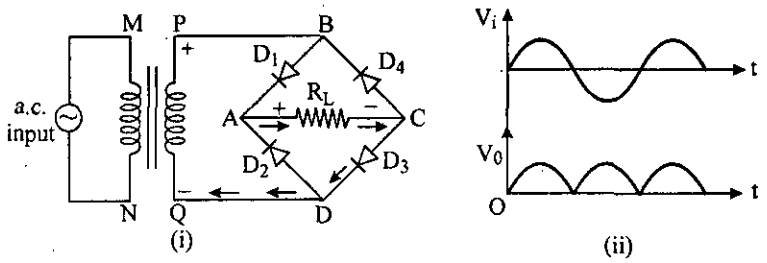


Fig 36.

Working : During the positive half cycle of the primary or secondary voltage, the end *P* becomes positive while the end *Q* becomes negative. This makes diodes D_1 and D_3 forward biased while diodes D_2 and D_4 reverse biased. Now the diodes D_1 and D_3 conduct current through the load resistance and are in series with it. Diodes D_2 and D_4 practically do not conduct the current. During the negative half cycle of the secondary voltage, end *P* of the bridge becomes negative while the end *Q* becomes positive. This makes diodes D_1 and D_3 reverse biased while the other two diodes D_2 and D_4 forward biased. Now D_2 and D_4 are in series with the load resistance R_L and conduct current through it in the same direction as during positive half cycle. Thus the output obtained across R_L is d.c.

Disadvantages : The full wave bridge rectifier suffers from the following disadvantages :

(i) It requires the use of four diodes.

(ii) During each half cycle, two diodes conduct current through the load resistance and form a series with it. Therefore, the internal resistance of the bridge rectifier is double of that of a centre tapped rectifier where only one diode is used.

• 2.22. FILTERING CIRCUITS

The output of a rectifier is unidirectional but pulsating. It contains both a.c. and d.c. components. The presence of a.c. component produces hum in the circuit and so it is undesirable. The remove the a.c. part of the output a filter circuit is used which *removes **(filters out)** the a.c. component and allows the d.c. component to flow through the load.* A filter circuit, generally a combination of inductors and capacitors, is connected between th rectifier and the load as shown in Fig. 37.

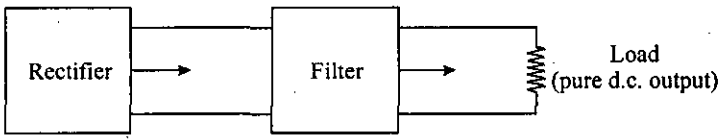


Fig.37.

Types of filter circuits : There are various types of the filter circuits. The most commonly used are : (i) capacitor filter (ii) choke input filter and (iii) capacitor input π-filter.

(i) Capacitor filter : Fig. 38 shows a capacitor filter circuit. A capacitor *C* is connected across the rectifier output and in parallel with load.

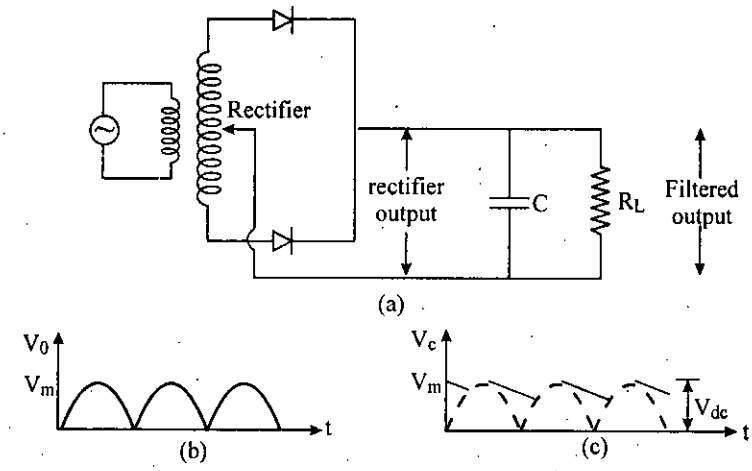


Fig. 38. (a) Full wave rectifier with capacitor filter, (b) Rectifier output (unfiltered) waveform, (c) Filtered output wave form.

Working principle : The basic principle of the capacitor filter is that a capacitor offers infinite reactance to d.c.($f = 0$)

$$X_C = \frac{1}{\omega C} = \frac{1}{2\pi fC} = \infty$$

and so it does not allow d.c. to pass through it. As the rectifier voltage increases, the a.c. component charges the capacitor while the d.c. component passes through the load. By the end of quarter cycle, the capacitor is charged to the peak value of the rectifier voltage. Now the rectifier voltage begins to decrease and the capacitor discharges through the load and the voltage across it decreases as shown in the figure. This decrease is very small as before the capacitor can fully discharge, the next positive voltage peak begins to recharge the capacitor. This section of charging and discharging continues and the output voltage with very little ripple left in it, is obtained. The output voltage is higher, its value being near the peak value of rectifier output voltage. The provide adequate filtering with the circuit, the reactance of the capacitor should be much lower than the load resistance. The capacitor filter circuit is preferred and commonly used for small load currents, because of its small size, low cost and good characteristics.

(ii) Choke input filter : It consists of a choke (inductance coil) and a capacitor. The choke is connected in series with the rectifier output and the capacitor across the load as shown in Fig. 39 (i) and (ii) represents the input and output waveform of the filter.

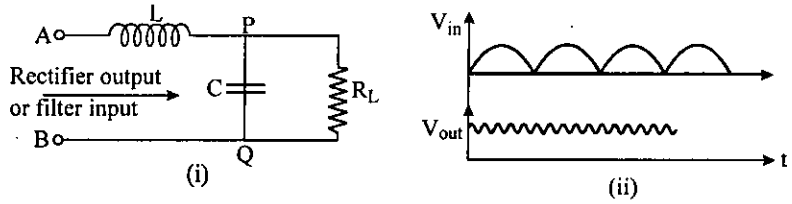


Fig. 39.

Working : The rectifier output which is pulsating in nature is applied across the terminals A and B of the filter circuit. The choke offers high reactance ($X_L = \omega L = 2\pi f L$) to the a.c. component while very low reactance to the flow of d.c. component. Thus practically whole of d.c. component along with the remaining part of a.c. component passes through the choke and reaches terminal P. The a.c. component is bye-passed by the filter capacitor due to the its low reactance and d.c. component reaches the load. Thus the output is practically d.c. Several identical sections may be used to improve the smoothing action.

Inductor filters are seldom used with half wave rectifier circuits, as the output voltage is very low compared with the average value of the rectified wave. With a full wave rectifier, it provides a steady output voltage even with a large load current variations.

π-filter or capacitor input filter : It consists of filter capacitor C_1 connected across the rectifier output, an inductance coil L in series and another filter capacitor C_2 connected across the load as shown in the Fig. 40 (i). Fig. 40 (ii) shows the filter input and output wave forms. The shape of the circuit containing C_1, L and C_2 appears like Greek letter π and hence this filter is also called π-filter.

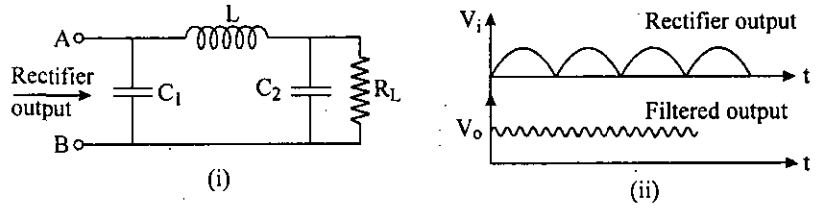


Fig. 40.

Working : The rectifier output is applied across the terminals 1 and 2 of the filter circuit. After the filtering process through the components C_1, L and C_2, the d.c. output appears across the load R_L. The filtering action of the three components is discussed as below :

The capacitor C_1 offers low reactance to a.c. component and infinite reactance to the d.c. component of the rectifier output. So most of the a.c. component is bypassed through C_1 and the remaining a.c. component and the whole of d.c. component reach the choke L which offers high reactance to a.c. component and almost zero reactance to the d.c. component. Thus the d.c. component flows through L. The filter capacitor C_2 bypasses the a.c. component which escapes the filtering through C_1 and L. Thus only d.c. component appears across the load R_L. Several identical filter sections may be used to improe further smoothing action. This filter circuit provides a higher output voltage than the choke input filter for higher rectifier peak current.

• 2.23. ZENER VOLTAGE REGULATOR

A semi-conductor diode which is designed to operate in the breakdown region without damage is known as **Zener diode.** In the breakdown region, an extremely small change in voltage causes very large variations in the current through the diode. In other words, the voltage across it is substantially constant for a large change of current through it. Due to this characteristics, it is used as a voltage regulator.

Operation *: The Fig. 41 shows the circuit of a zener diode regulator.* The unregulated output from the rectifier is applied across the zener diode through a seris resistance R. As long as the voltage V_{in} is grater than zener voltage V_Z, the zener operates in the breakdown region and maintains constant voltage across the load R_L. The resistance R limits the input current in the circuit. The zener maintains constant voltage across the load in spite of changes in load current or input voltage. This can be explained as follows. As the load current i_L increases, the zener current i_Z decreases so that the current through resistance R is constant. Now $V_{out} = V_{in} - iR$ and i is constant and hence the output voltage is constant. The reverse is also true. Again if the input voltage V_{in} increases, more current will flow through the zener, the voltage drop across R will increase in such a way that the load voltage remains constant. The reverse is also true.

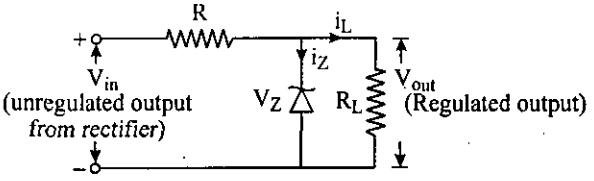


Fig. 41.

Limitatins : A zener regulator suffers from the following drawbacks :

(i) It has low efficiency for large load current as power loss in the series resistance R will be considerable.

(ii) The output voltage V_{out} changes slightly due to zener impedance ($V_{out} = V_Z + i_Z Z_Z$). Change in load current produces change in zener current.

Due to the above limitations, the use of zener regulator is limited only for such applications where variations in load current and input voltage are small.

• TEST YOURSELF

1. Explain the effect of temperature on the position of Fermi-level.

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2. What do you mean by diffusion ?

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3. Explain drift velocity and mobility.

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4. Define knee voltage.

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5. What is breakdown voltage ?

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6. Explain avalanche breakdown.

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7. Explain peak inverse voltage.

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8. Explain maximum power rating.

.....

.....

9. Show Fermi-levels for a *p-n* junction when it is zero biased, forward biased and reverse biased.

.....

.....

• EXERCISE

1. What do you understand by intrinsic and extrinsic semiconductors ? Derive expressions for the densities of free electrons and holes in an intrinsic semiconductor. Show that the Fermi level lies half way between the top of valence band and bottom of the conduction band.
2. State the law of mass action for intrinsic semiconductors. Discuss the temperature dependence of electron and hole concentrations.
3. What is the doping and extrinsic semiconductor ? Explain the mechanism of conduction in an extrinsic semiconductor.
4. Deduce an expression for the density of electrons in the conduction band of a *n*-type semiconductor and of holes in the valence band of *p*-type semiconductor.
5. Obtain the expressions for the electrical conductivity of an intrinsic and extrinsic semiconductors.
6. What is a *p-n* junction and junction diode ? Explain the formation of potential barrier in a *p-n* junction.
7. Discuss the behaviour of *p-n* junction under forward and reverse biasing. Explain the current flow and V-I characteristics in each biasing.
8. What is zener diode ? Explain its working and give its use.
9. Describe the principle and working of a tunnel diode.
10. Describe the working of light emitting diode (LED).
11. Explain the working of photo-diode.
12. Describe the working of Schottkey diode.
13. Describe solar cell. Explain the construction and principle of working of a silicon solar cell.

14. Explain static and dynamic characteristics of a *p-n* junction diode. What is load line of a diode circuit and how is it obtained ?
15. Describe the construction and working of a *p-n* junction diode as half wave rectifier. Derive the expressions for average and r.m.s. value of the output current, rectifier efficiency and ripple factor.
16. Explain the working of a *p-n* junction diode as a full wave rectifier. Obtain the expressions for its efficiency and ripple factor.
17. Explain the working of a full wave bridge rectifier.
18. *Why are filtering circuits used in power supplies ? Describe various types of the* filters.
19. Explain with a neat diagram, the action of a zener voltage regulator. What are its limitations ?
20. On increasing temperature, the conductivity of pure semiconductors :
    (a) decreases (b) increases
    (c) remains same (d) becomes zero
21. The mobility of free electron is greater than that the free holes because :
    (a) they are light
    (b) they carry negative charge
    (c) they require low energy to continue their motion
    (d) they mutually collide less
22. The resistance of a pure semiconductor is :
    (a) constant which decreases with temperature
    (b) constant which increases with temperature
    (c) constant and is independent of temperature
    (d) infinite at 0 K
23. The impurity element to be mixed in pure Ge to get *p-type semiconductor is* :
    (a) B (b) Bi (c) P (d) Sb
24. Th valency of impurity element for making donor type semiconductor will be :
    (a) 3 (b) 4 (c) 5 (d) None of these
25. The temperature coefficient of resistance of a semiconductor is :
    (a) negative (b) zero (c) positive (d) imaginary
26. In *N*-type semiconductors the electron concentration is equal to :
    (a) density of acceptor atoms
    (b) density of donor atoms
    (c) density of both type of atoms
    (d) independent on density of both type of atoms
27. The majority charge carriers of *p*-type semiconductor are :
    (a) only free holes (b) only free electrons
    (c) both (a) and (b) (d) neither (a) nor (b)
28. In *n*-type semiconductor, the Fermi energy level is situated :
    (a) just below the v.b. (b) just below the C.B.
    (c) just above the v.b. (d) in the middle of V.B. and C.B.
29. An intrinsic semiconductor is :
    (a) neutral (b) positively charged
    (c) negatively charged (d) none of these
30. Which out of the following is a semiconductor :
    (a) As (b) *P*
    (c) Al (d) Si
31. Which out of the following is not an impurity of *n*-type :
    (a) Sb (b) As
    (c) Al (d) Bi
32. The current in a semiconductor is due to the drifting of :

(a) free electrons (b) positive and negative ions
(c) protons (d) free electrons and holes

33. On increasing temperature of a semiconductor, its specific resistance will :
(a) decrease (b) increase (c) remain same (d) become zero

34. The resistivity of a semiconductor depends on :
(a) surface area of semiconductor
(b) length of semiconductor
(c) nature of atoms and size of path
(d) nature of atom of semiconductor

35. The band of maximum energy in which electrons are present is called :
(a) Valence band (b) Conduction band
(c) Fermi band (d) Forbidden band

36. The hole in a *p*-type semiconductor is :
(a) a donor level (b) an electron excess
(c) an electron deficiency (d) an atom deficiency

37. The stationary atom in *n*-type doped semiconductors is known as :
(a) donor atom
(b) acceptor atom
(c) sometimes donor and sometimes acceptor
(d) neither donor nor acceptor

38. The correct relation between n_i and P_i in an intrinsic semiconductor at ordinary temperature is :
(a) $n_i > P_i$ (b) $n_i < P_i$ (c) $n_i = P_i = 0$ (d) $n_i = P_i$

39. The relation between the number of free electrons in semiconductors (n) and its temperature (T) is :
(a) $n \propto T^{1/2}$ (b) $n \propto T$ (c) $n \propto T^{3/2}$ (d) $n \propto T^2$

40. The tunnel diode has :
(a) positive resistance
(b) negative resistance
(c) negative resistance at low temperature only
(d) positive as well as negative resistance

41. In a tunnel diode, there is :
(a) decrease of current with increase of voltage
(b) increase of current with increase of voltage
(c) anything can be there
(d) all the above

42. Zener diode can be used as :
(a) rectifier (b) transmitter (c) oscillator (d) voltage regulator

• ANSWERS

20. (b)	**21.** (c)	**22.** (d)	**23.** (a)	**24.** (c)	**25.** (a)
26. (b)	**27.** (a)	**28.** (b)	**29.** (a)	**30.** (d)	**31.** (c)
32. (d)	**33.** (a)	**34.** (d)	**35.** (a)	**36.** (c)	**37.** (a)
38. (d)	**39.** (c)	**40.** (b)	**41.** (a)	**42.** (d)	

U N I T - III

BIPOLAR TRANSISTORS

STRUCTURE

- Bipolar Junction Transistor
- Transistor Connections
- Common Emitter Configuration
- Relation Between α and β
- p-n-p Transistor in the Common Collector Configuration
- Various Features of the Three Transistor Configurations
- D.C. Load Line
- n-p-n Transistor in Common Base Configuration
- Transistor Biasing
- Inherent Variations of Transistor Parameters
- Essentials of a Transistor Biasing Circuit
- Hybrid Parameters
- Input Impedance
- h-Parameter of a CE Transistor Amplifier
- Cut Off Point, Saturation Point, Active Region and Power Rating of Transistor
- Merits of Transistor
- Base Region of a Transistor
  - Test yourself
  - Exercise
  - Answers

LEARNING OBJECTIVES

After learning this chapter, you will be able to know

- Study of bipolar junction transistor *i.e.*, n-p-n and p-n-p transistors in common base, common emitter and common collector configuration.
- Relationship between α and β *i.e.*, current gain in C.B. configuration and C.E. configuration.
- Study of D.C. load line.
- Methods of transistor biaring.
- Study of hybrid parameters use of these parameters in different configurations.
- Merits and demerits of transistors.

• 3.1. BIPOLAR JUNCTION TRANSISTOR

The bipolar junction transistor simply called the transistor is a three terminal solid state device for superior alternate to a vacuum triode used for achieving the amplification of weak signals. It was first discovered in 1948 by J. Bardeen and W. H. Brattain of U.S.A. Both holes and electrons take part in conduction of current in transistor and so it is called as a bipolar junction transistor abbreviated as BJT. A transistor transfers a signal from a low resistance to high resistance. The prefix 'trans' means the signal transfer property of the device while 'istor' classifies it in the resistors family'.

A transistor consists of two p-n junctions formed by sandwiching either p-type of n-type semiconductor between a pair of opposite types. There are two types of transistors:

(a) *p-n-p* transistor (b) *n-p-n* transistor

A transistor has three sections of doped semiconductors. The section on one side is the **emitter** and the section on the other side is **collector.** The middle section is called the **base** and forms two junctions between the emitter and collector.

Emitter : The emitter supplies majority charge carriers (holes or electrons) to its junction with the base and is always forward biased.

Collector : The collector collects the charges. It removes charges from its junction with the bse. It has a reverse bias and receives the charge carriers.

Base : The middle section which forms two *p-n* junctions between the emitter and collector is called the base. The base-emitter junction is forward biased offering low resistance for the emitter circuit. The base-collector junction is reverse biased offering high resistance in the collector circuit.

(a) *p-n-p* transistor : If a layer of *n*-type semi-conductor (silicon or germanium) is sandwiched between two layers of *p*-type semi-conductor, the device is known as *p-n-p* transistor. The middle layer is called base and the other two layers are called the emitter and the collector respectively, as shown in the figure 1. The base region is made extremely thin compared to the emitter and collector regions. Also the surface area of

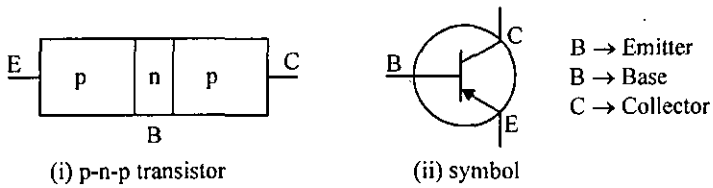


Fig. 1.

the emitter-base junction is made less than that of the collector-base junction. The arrow head represents the direction of current. The emitter-base junction works under forward bias and base-collector junction works under reverse bias.

(b) *n-p-n* transistor : If a layer of *p*-type semi-conductor (silicon or germanium) is sandwiched between two layers of *n*-type semi-conductor, the device is known as *n-p-n* transistor. The middle layer is called base and the other two layers are called the emitter and the collector respectively as shown in Fig. 2. The arrow head represents the

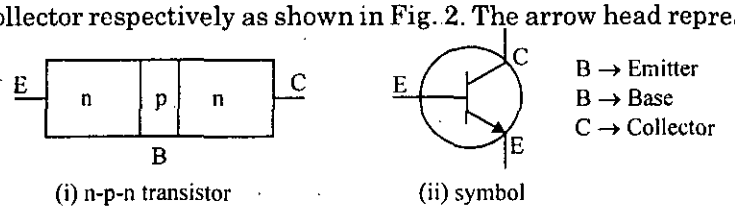


Fig. 2.

direction of current. The emitter-base junction works under forward bias and the base-collector junction works under reverse bias.

Working of *p-n-p* transistor : The Fig. 3 shows a basic circuit diagram of *p-n-p* transistor. A small forward bias is applied to the emitter-base junction while large reverse bias is applied to the base-collector junction. The forward bias of emitter-base junction causes the holes of the *p*-type emitter to flow towards the base, constituting the emitter current i_e. During their passage through the *n*-type base, they tend to combine with the electrons. The base lightly doped and very thin, only a few holes (less than 5%) combine with the electrons. The remaining more than 95% cross into the collector region constituting the collector current i_c. The electrons which combine with holes become valence electrons which flow down through holes into the external base lead constituting base current i_b. Thus we have,

$$i_e = i_c + i_b .$$

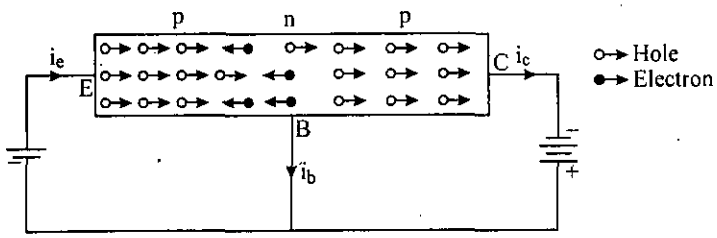


Fig. 3.

Working of *n-p-n* transistor : The Fig. 4 shows a basic *n-p-n* circuit diagram. The emitter-base junction is forward biased while the base-collector junction is reverse biased. The forward bias causes the electrons of the *n*-type emitter to flow towards the base, constituting the emitter current i_e. The base being very thin and lightly doped, only less than 5% electrons combine with the holes in the base region constituting the base current i_b and the remaining more than 95% electrons flow through the collector region constituting the collector current i_c.

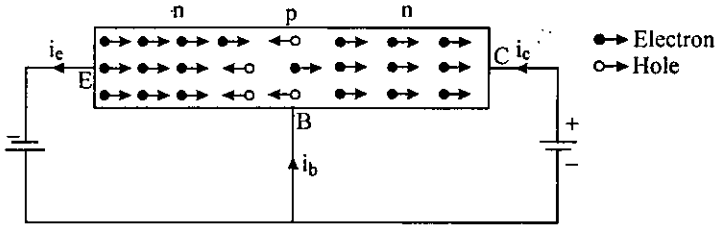


Fig. 4.

Again $$i_e = i_c + i_b$$

• 3.2. TRANSISTOR CONNECTIONS

The transistor has three leads-emitter, base and collector terminals whereas four terminals are required for the connection purpose, two for the input circuit and two for the output circuit. Therefore, one terminal is made common to both the input and output circuits. Accordingly, a transistor can be connected in a circuit in the following three modes :

(a) Common base configuration

(b) Common emitter configuration

(c) Common collector configuration.

Common base configuration : The Fig. (5) shows a *p-n-p* transistor connected in common base configuration. The base is commonly connected to the emitter and collector. The input in applied between emitter and base and the output is taken from collector and base. Ammeters and voltmeters are connected to measure the input and output voltage and current as shown in the figure.

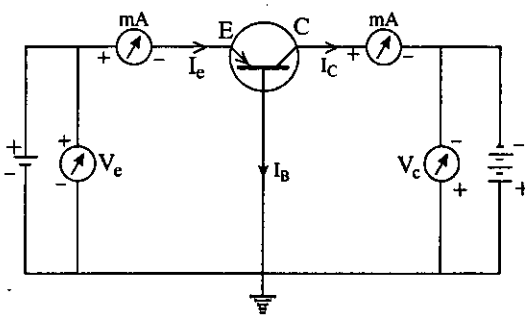


Fig. 5.

Input characteristics : The input characteristic curves are drawn between the various values of the emitter voltage v_e and the corresponding values of the emitter current i_e, the collector voltage v_c being kept constant. The curves obtained for two different values of collector voltage v_{c_1} and v_{c_2} are as shown in the Fig. 6. Obviously for a certain value of collector voltage v_c the emitter current i_e rises rapidly with small change in emitter voltage v_e. These characteristics also show a cut-in or threshold voltage, below which the emitter current is very small. It is also obvious from the curves

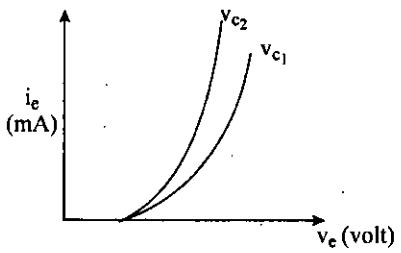


Fig. 6.

that the emitter current is almost independent of collector-base voltage. The input resistance r_i given by $r_i = \frac{\partial v_e}{\partial i_e}$ at constant v_e is very small of the order of few ohms.

Output characteristics : The output characteristic curves are drawn between the different valus of collector voltage v_c and the corresponding values of the collector current i_c keeping emitter current i_e as constant. It is clear from these curves that there is variation in the collector current at low values of collector voltage. Beyond this, there is no appreciable increase in current with the increase in collector voltage *i.e.*, the collector current is practically independent of the collector voltage. It is also clear from the curves that a very large change in the collector voltage produces a very small change in collector current. In other words the output resistance of the transistor given by $r_0 = \frac{\partial v_c}{\partial i_c}$ at constant i_e is very high of the order of several tens of kilo ohms.

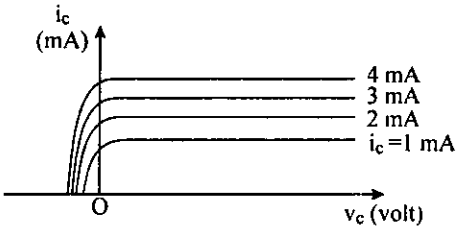


Fig. 7.

Current transfer characteristics : The current transfer characteristic is obtained by plotting different values of emitter current i_e and collector current i_c keeping collector voltage v_c constant as shown in Fig. 8.

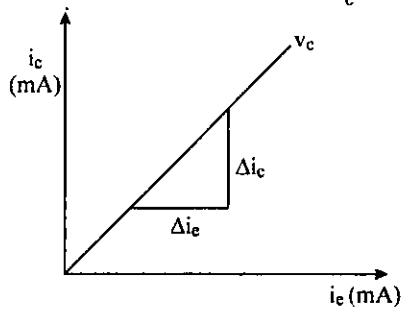


Fig. 8.

The slope $\left(\frac{\Delta i_c}{\Delta i_e}\right)$ of the curve gives the current gain α of a transistor for the given values of i_b and v_c.

The current gain of a common base transistor circuit is defined as the ratio of the change in collector current to the change in emitter current at a constant collector voltage

$$\alpha = \left(\frac{\Delta i_c}{\Delta i_e}\right)_{v_c}$$

The value of α is slightly less than 1.

• 3.3. COMMON EMITTER CONFIGURATION

The Fig. 9 shows a *p-n-p* transistor connected in common emitter configuration. The emitter is commonly connected to the base and collector. The input is applied between base and emitter and the output is derived from the collector and emitter. The ammeters and voltmeters are connected to measure input and output current and voltage as shown in the figure.

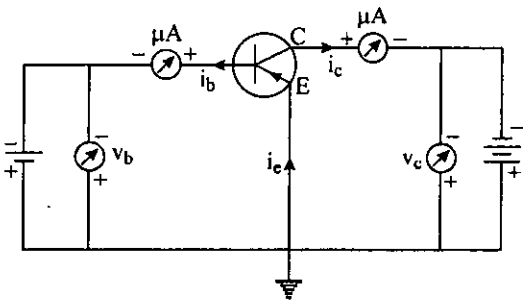


Fig. 9.

Input characteristics : The input characteristic curves are drawn between base voltage v_b and base current i_b keeping v_c as constant. The input characteristics are similar to that for the common base configuration. Obviously the base current (μA) varies non-linearly with the base voltage as shown in the Fig. 10. These characteristics also define the threshold voltage. The input resistance

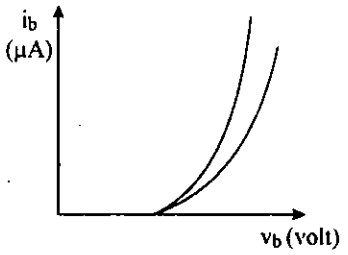


Fig. 10.

$\left(r_i = \frac{\Delta v_b}{\Delta i_b} \text{ at constant } v_c\right)$ is hgiher than that in common base configuration. The value is of the order of few hundred ohms.

Output characteristics : The output characteristic curves are drawn between the collector voltage v_c and the collector current i_c keeping i_b as constant. The curves are obtained as shown in the Fig. 11. The curves are not parallel to the v_c axis. This shows that the collector current is affected by the collector voltage v_c which is not the case for the common base configuration. Also there is some collector current even for the zero base current. This current is called common emitter leakage current. The output resistance r_0 defined by $\frac{\Delta v_c}{\Delta i_c}$ at constant i_b is less than that of common base circuit. It is of the order of 50 KΩ.

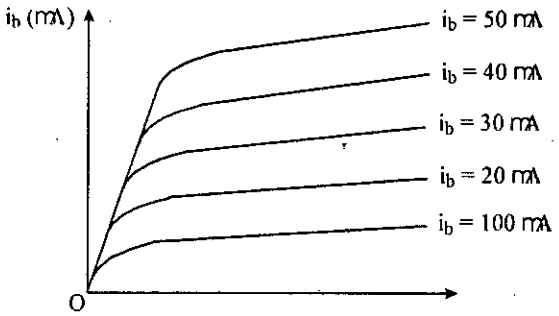


Fig. 11.

Current transfer characteristics : The current transfer characteristic curve is obtained by plotting i_b versus i_c keeping v_c constant as shown in the Fig. 12. The slope $\frac{\Delta i_c}{\Delta i_b}$ of the curve gives the current gain β of the transistor for the given values of i_b and v_c.

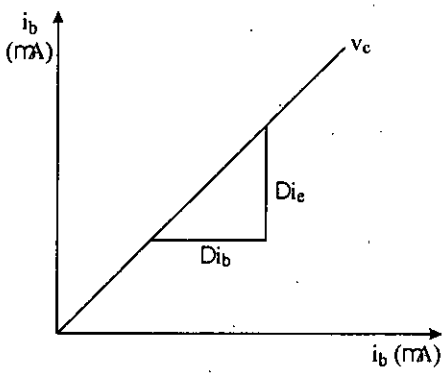


Fig. 12.

The current gain of a common emitter configuration is defined as the ratio of the change in collector current to the change in base current keeping collector voltage constant.

$$\beta = \left(\frac{\Delta i_c}{\Delta i_b}\right)_{v_c}$$

The value of β is nearly equal to 50 for a typical transistor.

• 3.4. RELATION BETWEEN α AND β

We know that $$\alpha = \left[\frac{\Delta i_c}{\Delta i_e}\right]_{v_c} \quad ...(i)$$

and $$\beta = \left[\frac{\Delta i_c}{\Delta i_b}\right]_{v_c} \quad ...(ii)$$

Eqn. (ii) can be written as

$$\beta = \frac{\Delta i_c}{\Delta i_e} \times \frac{\Delta i_e}{\Delta i_b} = \alpha \frac{\Delta i_e}{\Delta i_b} \quad ...(iii)$$

We know that

$$i_e = i_b + i_c$$

$$\therefore \quad \Delta i_e = \Delta i_b + \Delta i_c$$

or $$\frac{\Delta i_e}{\Delta i_b} = 1 + \frac{\Delta i_c}{\Delta i_b} = 1 + \beta \quad \text{(from eqn. (ii))}$$

Putting this value in eqn. (iii),

$$\beta = \alpha (1 + \beta) = \alpha + \alpha\beta$$

or $$\beta (1 - \alpha) = \alpha$$

or

$$\beta = \frac{\alpha}{1 - \alpha}$$

This is the relation between α and β. Since α is nearly equal to one so $1 - \alpha$ is very small and hence β is very large.

• 3.5. n-p-n TRANSISTOR IN THE COMMON COLLECTOR CONFIGURATION

The Fig. 13 shows a *p-n-p* transistor connected in common collector configuration. The collector is commonly connected to the base and the emitter. The input is applied between base and collector and the output is derived from the emitter and the collector. The ammeters and voltmeters are connected to measure the input and output current and voltage as shown in the figure.

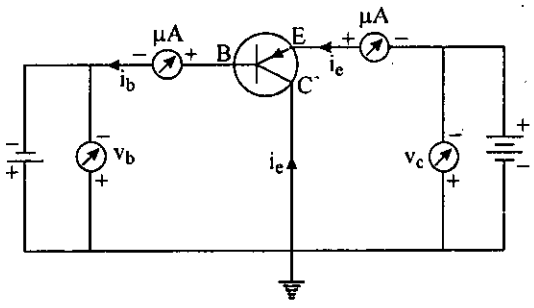


Fig. 13.

Current amplification factor γ : The current gain or amplification factor γ is defined as **the ratio of change in emitter current to the change in base current, keeping emitter voltage constant**

$$\gamma = \left(\frac{\Delta i_e}{\Delta i_b}\right)_{v_e}$$

The amplification in this configuration is nearly the same as in the common emitter configuration as $\Delta i_e \simeq \Delta i_c$.

Relation between α and γ

We have $$\gamma = \frac{\Delta i_e}{\Delta i_b} \quad \text{...(i)}$$

and $$\alpha = \frac{\Delta i_c}{\Delta i_e} \quad \text{...(ii)}$$

Now $$i_e = i_b + i_c$$

$\therefore$ $$\Delta i_e = \Delta i_b + \Delta i_c$$

or $$\Delta i_b = \Delta i_e - \Delta i_c$$

Substituting the value of Δi_b in eqn. (i)

$$\gamma = \frac{\Delta i_e}{\Delta i_e - \Delta i_c}$$

$$= \frac{1}{1 - \frac{\Delta i_c}{\Delta i_e}}$$ (dividing numerator and denominator by Δi_e)

or $$\gamma = \frac{1}{1 - \alpha}$$ [from eqn. (ii)]

Application : The common collector configuration has very high input resistance and very low output resistance. So the voltage gain is always less than unity. Therefore, this configuration is not generally used for amplification. However, this is primarily used for impedance matching.

• 3.6. VARIOUS FEATURES OF THE THREE TRANSISTOR CONFIGURATION

The comparison of various features of transistor configurations is given below in tabular form :

S. No.	Characteristic	Common base	Common emitter	Common collector
1.	Input resistance	Low (nearly 100 Ω)	Low (nearly 750 Ω)	Very high (nearly 750 kΩ)
2.	Output resistance	Very high (nearly 500 kΩ)	High (nearly 50 kΩ)	Low (nearly 50 Ω)
3.	Current gain	Less than unity	Ranges from 20 to 500	Ranges from 25 to 500
4.	Voltage gain	Nearly 150	Nearly 500	Less than unity
5.	Applications	For high frequency	For audio frequency	For impedance matching

Commonly used configuration : There are three transistor configurations *viz.*, the common base, common emitter and common collector configurations. Out of these three, the commonly used configuration is the common emitter configuration. It is used in nearly 90% of all transistor applications. This is due to the following special characteristics :

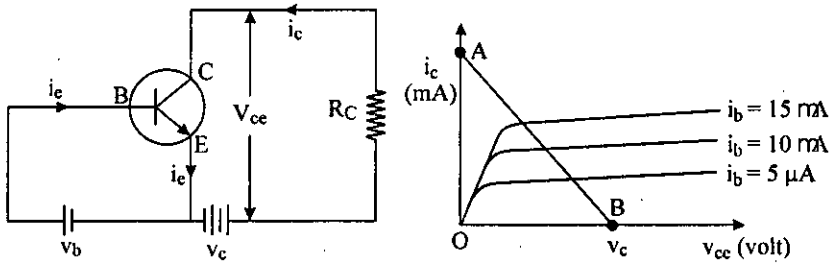
(i) High current gain : The current gain β in common emitter configuration is very large. It ranges from 20 to 500.

(ii) High voltage and power gain : Due to very large current gain, this configuration has very large voltage and power gain.

(iii) Impedance ratio : The ratio of the output impedance to the input impedance is moderate (about 50) whereas in other configurations, the ratio is very large. Therefore, the common emitter configuration is best one for coupling between various transistor stages.

• 3.7. D.C. LOAD LINE

The collector current for various collector-emitter voltages is generally required in the transistor circuit analysis. One of the methods is to plot the output characteristics and find the collector current. Another convenient and generally used method is known as **'load line method'**. The Fig. 14 shows the circuit of a common emitter *n-p-n* transistor when no signal is applied to the input circuit (base-emitter), the output



characteristics obtained are shown in the figure.

Fig. 14.

Load line analysis : The value of the collector emitter voltage v_{ce} at any instant is given by

$$v_{ce} = v_c - i_c R_c \qquad ...(i)$$

The eqn. (i) represents a straight line, as v_c and R_c are constant. This can be represented by a straight line on the output characteristics. This is known as **d.c. load line.** To draw this load line, we find the points *A* and *B* as follows :

(i) When the collector current $i_c = 0$, the collector-emitter voltage v_{ce} is maximum and equal to v_c.

Putting $i_c = 0$ in eqn. (i), we get

$$v_{ce} = v_c$$

This gives the point $B\,(OB = v_c)$ on the collector-emitter voltage axis.

(ii) When the collector-emitter voltage $v_{ce} = 0$, the collector current $i_c = \frac{v_c}{R_c}$ is maximum.

Putting $v_{ce} = 0$ in equation (i)

$$i_c = \frac{v_c}{R_c}$$

This gives the point $A\left(OA = \frac{v_c}{R_c}\right)$ on the collector current axis.

The line AB joining the points A and B is the **d.c. load line.** The line is so called as the resistance R_c is the load resistance.

Importance : The various values of the current i_c and voltage v_{ce} can be obtained from the load line. Thus the behaviour of the transistor amplifier can be investigated by the load line.

• 3.8.(I) n-p-n TRANSISTOR IN COMMON BASE CONFIGURATION

The fig. 15 shows a *n-p-n* transistor connected in common base configuration.

The characteristic curves obtained are similar to that of *p-n-p* common base transistor configuration.

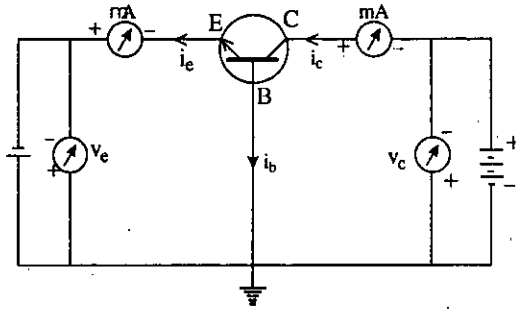


Fig. 15.

(ii) *n-p-n* transistor in common emitter configuration : The Fig. 16 shows a *n-p-n* transistor connected in common emitter configuration.

The characteristic curves obtained are similar to that of a *p-n-p* common emitter transistor configuration.

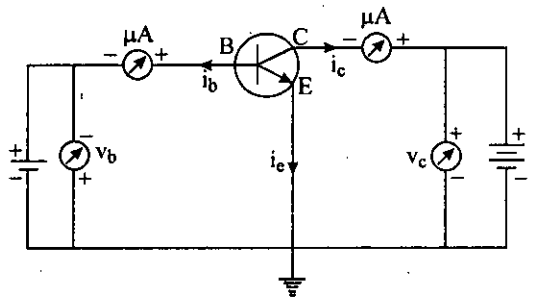


Fig. 16.

(iii) *n-p-n* transistor in common collector configuration : The fig. 17 shows a *n-p-n* transistor connected in common collector configuration.

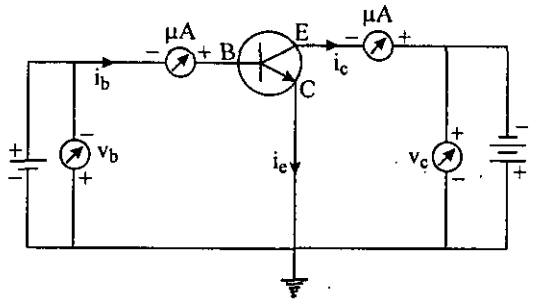


Fig. 17.

The characteristic curves obtained are similar to that obtained in case of a *p-n-p* common collector transistor.

• 3.9. TRANSISTOR BIASING

Basically, the transistor is used to amplify a weak signal given to its input circuit. It is desired that in the amplified output the magnitude of the signal should increase without any change in signal shape. This is achieved by providing means to ensure that input circuit of the transistor remains forward biased and output circuit remains reverse biased during all parts of the signal. This is known as **transistor biasing.** Transistors are used in variety of circuits *e.g.,* amplifiers, switches, logic circuits etc. Depending upon the particular application, the transistors are given proper biasing so that they can operate in the desired region of their characteristics. This can be achieved with a bias battery or associating a circuit with a transistor. The circuit which provides transistor biasing is known as biasing circuit. The biasing must ensure (i) proper zero signal collector current (ii) proper base-emitter voltage at any instant and (iii) proper collector-emitter voltage at any instant.

The proper flow of zero signal collector current and the maintenance of proper collector-emitter voltage during the passage of signal is known as transistor biasing.

Quiescent point (Q-point): The Quiescent point or the operating point of a transistor represents a point on the transistor characteristics, which has the desired values of the current and the voltage.

The zero signal values of i_c and v_{ce} are known as the operating point. It is called operating point because the variations of i_c and v_{ce} take place about this point when signal is applied. It is also called **Quiescent (silent) point,** as it is the point on $i_c - v_{ce}$ characteristic in the absence of the signal *i.e.,* the transistor is silent. The Q-point is selected with the help of biasing technique. There are certain following factorw which should be taken into account while selecting an operating point.

(a) The transistors have to be operated within the maximum limits for the current, the voltage and the power to avoid any damage to it. Therefore, the operating point is selected so that the transistor does not cross the maximum ratings during the passage of the input signal.

(b) The positive and the negative parts of the input signal change the voltage and the current of the transistor. The operating point should, therefore, be so selected that the input signal should not drive the transistor into the cut-off or the saturation region.

(c) The operating point must be selected in such a way that the entire input signal is covered in the linear region of the characteristics, so that the gain remains constant.

(d) The operating point must be stabilized against the temperature variation.

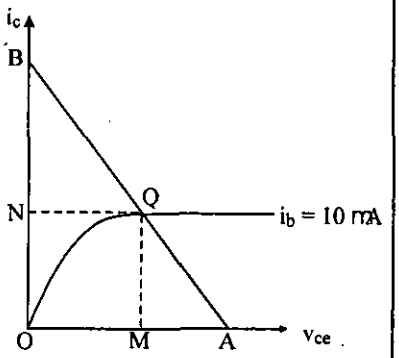


Fig. 18.

Location of operating point : The operating point is located by determining the zero signal values of i_c and v_{ce}. The method is as follows. The transistor characteristic is drawn between v_{ce} and i_c keeping i_b (say 10 μA) as constant. Again the load line AB is drawn meeting the characteristics at the point Q which is the desired operating point. The point Q is described by

$$v_{ce} = OM \text{ volt}$$
$$i_c = ON \text{ mA}$$

Thus the operating pint is determined by the intersecting point of the load line and the proper base current curve.

• 3.10. INHERENT VARIATIONS OF TRANSISTOR PARAMETERS

Generally, the transistor parameters are not the same for every transistor even of the same type. As an example the value of current gain β for a silicon *n-p-n* transistor varies from 100 to 600 for the same type of the transistor. These variations are due to the manufacturing techniques (one factor is to control base width which may vary though slightly). The inherent variations of transistor parameters may change the operating point. It is therefore, necessary that biasing network be so designed that it should be able to work with all transistors of one type.

Stabilisation : When the temperature changes or the transistor is replaced, the operating point changes. But it is desired that the operating point should remain fixed *i.e.*, the operating pint should be independent of the variations. This is known as **stabilisation.**

The stabilisation is the process of making operating point independent of temperature changes or variations in transistor parameters.

Necessity of stabilisation : The stabilisation of the operating point is necessary for the following reasons :

(i) Temperature dependence of collector current.

(ii) Individual variations and

(iii) Thermal runway.

(i) Temperature dependence of i_c : The collector leakage current is greatly influenced by temperature changes which in turn changes the collector current i_c which is undesired. Therefore, the stabilisation of the operating point is necessary.

(ii) Individual variations : Even the same type of transistors may have different values of parameters *i.e.*, the values of β and v_{be}. When a transistor is replaced by another of even the same type, the operating pint changes. Therefore, it becomes necessary to stabilise it *i.e.*, to hold i_c constant irrespective of the individual variations.

(iii) Thermal runway : The flow of collector current develops heat within the transistor. This raises the transistor temperature which in turn increases the collector leakage current. This inturn increases the collector current thereby increasing the transistor temperature. Thus this effect multiplies and the collector current may become so large as to damage the transistor. This is known as **thermal runway.** This necessities the stabilisation.

• 3.11. ESSENTIALS OF A TRANSISTOR BIASING CIRCUIT

We know that for faithful amplification, the transistor biasing is necessary. The transistor biasing circuit should be so designed as to meet the following conditions :

(a) It should maintain proper zero signal collector current.

(b) It should ensure the stabilisation of operating point.

(c) It should ensure that the base-emitter voltage v_{be} should not fall below the potential barrier 0.5 volt for germanium and 0.7 volt for silicon transistor at any instant.

(d) It should also ensure that the collector-emitter voltage v_{ce} should not fall below the knee voltage 0.5 V for Ge transistors and 1 V for Si transistors at any instant.

Method of transistor biasing : Generally, the transistor biasing was done with two separate batteries for input and output circuits. It is desirable in the interest of simplicity and economy that there should be a single source of supply, there are the following commonly used methods of transistor biasing :

(a) Base resistor method

(b) Feedback resistor method and

(c) Voltage divider method.

(a) Base resistor method : A constant base current bias circuit or a fixed bias circuit is shown in the Fig. 19. The circuit shows only one power supply which provides both the forward and reverse bias conditions. A high resistance R_b (several hundred (kΩ) is connected between base and positive end of supply for n-p-n transistor. The base is at a positive potential with respect to the common emitter. Thus the base-emitter junction is forward biased. The collector-base junction becomes reverse biased if the collector is made more positive than the base. This achieved with the help of resistor R_l whose value is selected at less than that of R_b. The value of R_b can be shown to be given by

$$R_b = \frac{V_{cc} - V_{be}}{i_b}$$

Since $V_{be} << V_{cc}$

so $$R_b \simeq \frac{V_{cc}}{i_b}$$

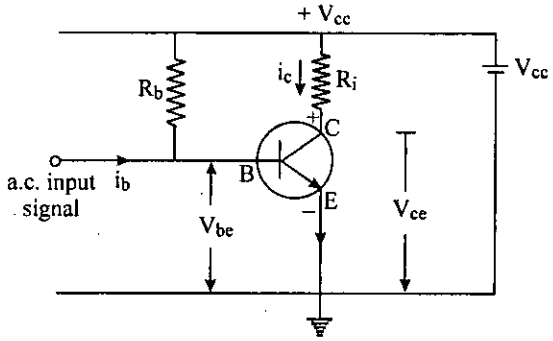


Fig. 19.

Again since V_{cc} is fixed value and i_b is choosen at some suitable value, so the value of R_b is constant. Hence this method is also known as **fixed bias method.**

Merits : (i) The biasing circuit is very simple. It requires one resistance R_b only.

(ii) The biasing conditions can easily be set and the value of R_b can be determined directly by simple calculations.

(iii) Since no register is used across the base emitter junction, so there is no loading of the source.

Demerits : (i) The stabilisation in this method is poor, as there is no means to check increase in collector current due to temperature rise and individual variations.

(ii) The chances for thermal runway are strong as the stability factor is very high.

This method of biasing is not generally used due to the above demerits.

(b) Feed-back resistor method : The circuit for the feed back resistor method is shown in the Fig. (20). The required value of R_b can be shown to be given by

$$R_b = \frac{V_{cc} - V_{be}}{i_b} \quad \text{where } i_b = \frac{i_c}{\beta}$$

The R_b can be determined directly

Merits : (i) This circuit is also simple.

(ii) This circuit provides a negative feedback and so the gain of the amplifier is reduced.

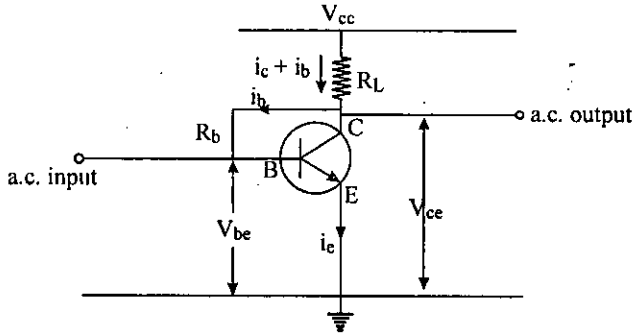


Fig. 20.

Demerits : (i) The circuit does not provide fair stabilisation, as the stability factor is fairly high, though lesser than that of fixed bias.

(ii) This circuit provides a negative feedback and so the gain of the amplifier is reduced.

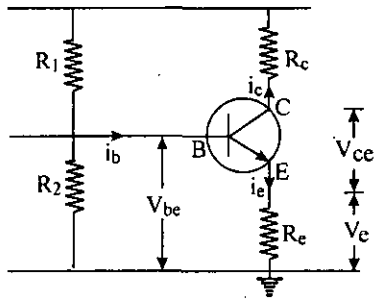


Fig. 21.

(c) Voltage divider bias method : The fig. 21 shows the voltage divider bias method, which is a most widely used method for biasing and stabilisation to a transistor. This involves the use of two resistors R_1 and R_2 connected across the supply voltage V. Resistors R_1 and R_2 forms the voltage divider. The voltage V_2 across R_2 is he forward bias of the base-emitter junction.

This can be shown that the emitter current is given by

$$i_e = \frac{V_2 - V_{be}}{R_e}$$

Since $i_e \simeq i_c$

$$\therefore \quad i_c \simeq \frac{V_2 - V_{be}}{R_e}$$

Obviously i_c does not depend upon β.

Again $V_2 >> V_{be}$, so $i_c = \frac{V_2}{R_e}$ is almost independent of the transistor parameters and hence good stabilisation is achieved.

Merits : (i) Due to excellent stabilisation, this method is most widely used and has become universal method for transistor biasing.

(ii) The stability factor is minimum (1–10) and so leads to the maximum possible thermal stability.

Demerits : This method reduces the gain β because it provides shunt path for the input signal. But this reduction in the gain is accepted because of the excellent stabilisation provided by the method.

• 3.12. HYBRID PARAMETERS

The behaviour of a transistor amplifier can be predicted by knowing its operating characteristics *e.g.*, input impedance, output impedance, gain etc. These characteristics are determined exactly by knowing four parameters of a transistor measured experimentally. These are called hybrid or *h*-parameters of the transistor and can be measured very easily.

Every linear circuit having input and output terminals can be analysed by four parameters called hybrid or h-parameters (linear circuit is one in which its elements, resistances, inductances, capacitances remain fixed while the voltage across them changes).

Dimensions of *h*-parameters : There are four *h*-parameters out of them, one is measured in ohm, one in mho and the other two are dimensionless.

Since these parameters have mixed dimensions and hybrid means **'mixed'** so the parameters are called **hybrid parameters.**

Let us consider a linear circuit shown in the fig. 22. Let the input voltage and current are v_1 and i_1 and the output voltage and current are v_2 and i_2 respectively. It can be shown by advanced circuit theory that the voltages and currents can be related by the following sets of equations :

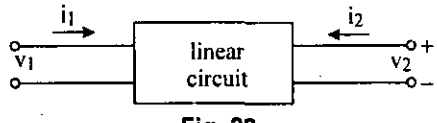


Fig. 22.

$$v_1 = h_{11} i_1 + h_{12} v_2 \quad \text{...(i)}$$
$$i_2 = h_{21} i_1 + h_{22} v_2 \quad \text{...(ii)}$$

In the above equations the h_{11} etc. are constants for the circuit and are called h-parameters. From the equations, it is obvious that h_{11} has the dimensions of impedance (ohm), h_{12} and h_{21} are dimensionless and h_{22} has the dimensions of admittance (mho).

Thus for every linear circuit, there are four h-parameters. One having dimensions of ohm, one of mho and two dimensionless. These h-parameters of a given circuit are constant and are different for different circuits.

Determination of h-parameters : The use of h-parameters is due to the relative ease with which they can be measured. The h-parameters of the circuit shown above can be determined in the following way :

(a) If the output terminals are short circuited, then $v_2 = 0$. Putting this value in eqns. (i) and (ii), we have

$$v_1 = h_{11} i_1 \quad \text{so} \quad h_{11} = \frac{v_1}{i_1} \quad \text{(ohm)}$$

and

$$i_2 = h_{21} i_1 \quad \text{so} \quad h_{21} = \frac{i_2}{i_1} \quad \text{(dimensionless)}$$

h_{11} represents the input impedance and h_{21} represents the current gain with output shorted.

(b) If the input terminals are open that is the input current i_1 is zero, then from eqns. (i) and (ii), we get

$$v_1 = h_{12} v_2 \quad \text{so} \quad h_{12} = \frac{v_1}{v_2} \quad \text{(dimensionless)}$$

and

$$i_2 = h_{22} v_2 \quad \text{so} \quad h_{22} = \frac{i_2}{v_2} \quad \text{(mho)}$$

Now h_{12} is a ratio of input and output voltages, it is dimensionless and is called **feedback ratio with input terminals open.** h_{22} is the ratio of output current and output voltage and so describes the admittance and is called **output admittance with input terminals open.**

• 3.13. INPUT IMPEDANCE

Let us consider a general linear circuit with input and output shown in the figure 23. R_L is the load resistance connected across the output terminals. The input impedance which is defined as the ratio of input voltage to input current is given by

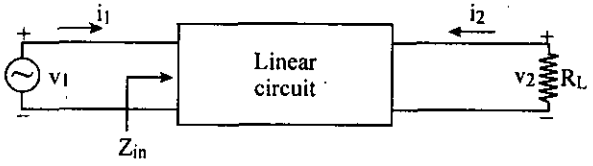


Fig. 23.

$$Z_{in} = \frac{v_1}{i_1}$$

Putting the values of $v_1 = h_{11} i_1 + h_{12} v_2$, we get

$$Z_{in} = \frac{h_{11} i_1 + h_{12} v_2}{i_1} = h_{11} + \frac{h_{12} v_2}{i_1} \quad \text{...(iii)}$$

Again $i_2 = h_{21} i_1 + h_{22} v_2$ and from the figure $i_2 = -\frac{v_2}{R_L}$. i_2 is negative because the current in the load is opposite to that shown in the figure 23.

$$\therefore \quad -\frac{v_2}{R_L} = h_{21} i_1 + h_{22} v_2$$

or $$-h_{21}i_1 = h_{22}v_2 + \frac{v_2}{R_L} = \left(h_{22} + \frac{1}{R_L}\right)v_2$$

$$\frac{v_2}{i_1} = -\frac{h_{21}}{h_{22} + \frac{1}{R_L}} \quad \text{...(iv)}$$

Putting the value of $\frac{v_2}{i_1}$ in (iii), we get

$$Z_{in} = h_{11} - \frac{h_{12}h_{21}}{h_{22} + \frac{1}{R_L}}$$

This is the expression for the input impedance of a linear circuit in terms of h-parameters. If either h_{12} or R_L is very small, the input impedance because

$$Z_{in} = h_{11}(\text{The second term is neglected})$$

(ii) Current gain : The current gain A_i of the circuit is given by

$$A_i = \frac{i_2}{i_1}$$

From eqn. (ii), $i_2 = h_{21}i_1 + h_{22}v_2$

and $$v_2 = -i_2R_L$$

$\therefore$ $$i_2 = h_{21}\,i_1 - h_{22}\,i_2\,R_L$$

or $$i_2\,(1 + h_{22}R_L) = h_{21}\,i_1$$

or $$\frac{i_2}{i_1} = \frac{h_{21}}{1 + h_{22}R_L}$$

With this value, the current gain A_i in terms by h-parameters is

$$A_i = \frac{h_{21}}{1 + h_{22}R_L}$$

If $h_{22}R_L << 1$, then $A_i \simeq h_{21}$.

Voltage gain : The voltage gain A_v of the circuit is given by

$$A_v = \frac{v_2}{v_1}$$

Now $$v_1 = i_1Z_{in} \text{ so}$$

$$A_v = \frac{v_2}{i_1Z_{in}}$$

Putting the value of $\frac{v_2}{v_1}$ from eqn. (iv), we have

$$A_v = -\frac{h_{21}}{Z_{in}\left(h_{22} + \frac{1}{R_L}\right)}$$

This is the expression of voltage gain for a linear circuit in terms of h-parameers.

• 3.14. *h*-PARAMETERS OF A CE-TRANSISTOR AMPLIFIER

The fig. 24 shows a simple circuit for a CE transistor amplifier. The eqns. for the h-parameters are

$$v_1 = h_{11}i_1 + h_{12}v_2$$
$$i_2 = h_{21}i_1 + h_{22}v_2$$

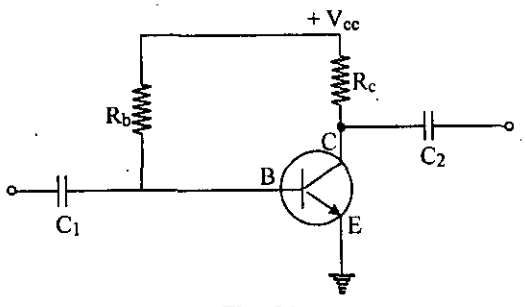


Fig. 24.

Using standard transistor nomenclature, the above eqns. are rewritten as

$$v_{be} = h_{ie}\, i_b + h_{re}\, v_{ce} \quad ...(i)$$

$$i_c = h_{fe} i_b + h_{oe}\, v_{ce} \quad ...(ii)$$

where $h_{11} = h_{ie}$ represents input impedance of *CE* transistor

$h_{12} = h_{re}$ represents reverse voltage feedback ratio

$h_{21} = h_{fe}$ represents forward current transfer ratio

$h_{22} = h_{oe}$ represents output admittance

Subscript *e* stands for *CE* transistor.

Determination h_{ie} and h_{fe} : To determine these parameters, the output is a.c. short circuited as shown in the fig. 25. This is achieved by making C_2 very large. Therefore, the changing component of collector current flows through C_2 instead of R_c and a.c. voltage developed across C_2 is zero *i.e.*, $v_{ce} = 0$.

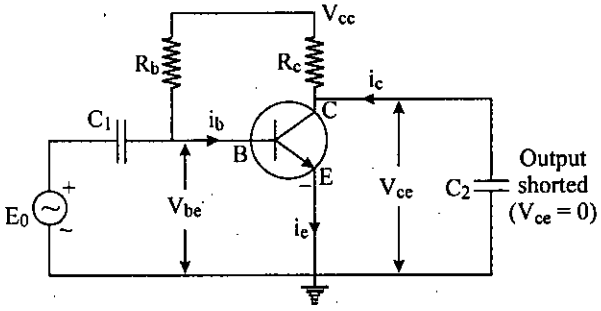


Fig. 25.

Putting $v_{ce} = 0$ in eqns. (i) and (ii), we get

$$v_{be} = h_{ie}\, i_b \quad \text{and} \quad i_c = h_{fe}\, i_b$$

$$\therefore \quad h_{ie} = \frac{v_{be}}{i_b} \quad \text{and} \quad h_{fe} = \frac{i_c}{i_b} \qquad \text{for } v_{ce} = 0$$

Thus the two parameters are determined.

Determination of h_{re} and h_{oe} : To determine these parameters, the input is a.c. open circuited as shown in the Fig. (26).

A signal generator is applied across the output and the resulting V_{be}, V_{ce} and i_c are measured. A large inductance L is connected in series with R_b. Due to negligible resistance, it does not affect the operating point and due to large reactance, the a.c. can not flow through R_b. This means that the base is effectively open circuited *i.e.*, $i_b = 0$.

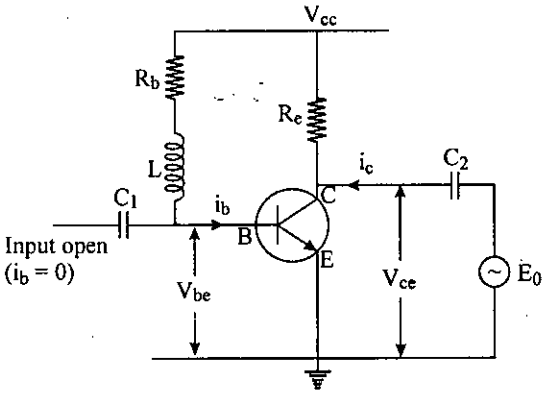


Fig. 26.

$$V_{be} = h_{re} V_{ce} \quad \text{or} \quad h_{re} = \frac{V_{be}}{V_{ce}}$$

and $$i_c = h_{oe}\, V_{ce} \quad \text{or} \quad h_{oe} = \frac{i_c}{V_{ce}} \qquad \text{for } i_b = 0$$

Thus the two parameters are determined.

Limitations of *h*-parameters : The *h*-parameters provide accurate information regarding current gain, voltage gain, input and output impedances of a transistor amplifier. However, this approach suffers from the following drawbacks :

(i) It is difficult to find exact values of *h*-parameters for a transistor due to temperature and operating point variations.

(ii) The use of *h*-parameters gives correct results for small a.c. signals only, as a transistor behaves as a linear device for small signals only.

• 3.15. CUT OFF POINT, SATURATION POINT, ACTIVE REGION AND POWER RATING OF TRANSISTOR

The performance of transistor amplifier depends upon its various parameters which change according to its mode of operation. As common emitter configuration is universally used, the terms are explained in reference of this configuration. The figure below shows a transistor circuit and the output characteristics along with the d.c. load line.

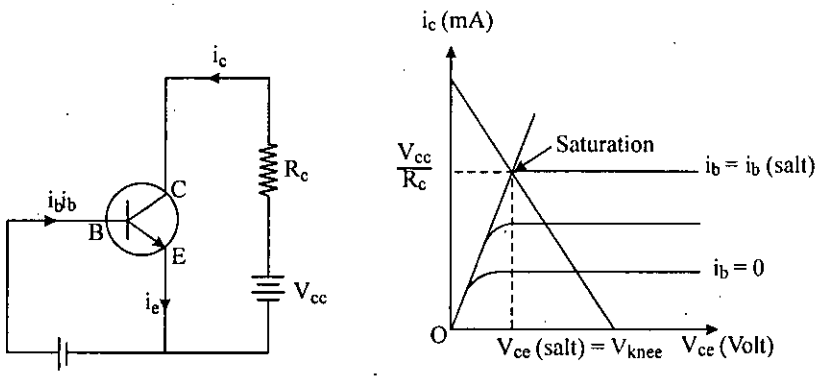


Fig. 27.

(a) Cut-off point : The cut-off point is the point where the load line intersects the $i_b = 0$ curve. At this point, only a small collector current exists and the base-emitter junction no longer remains forward biased and normal transistor action fails. The collector-emitter voltage is nearly equal to V_{cc}.

(b) Saturation point : It is the point at which the load line intersects $i_b = i_b$ (sat) curve. At this point, the base current is maximum and so is the collector current. At saturation, collector-base junction no longer remains reverse biased and normal transistor action fails.

(c) Active region : The region between cut-off and saturation is known as **active region.** In the active region, collector base junction remains reverse biased. While base-emitter junction remains forward biased and the transistor functions normally. The proper biasing is provided to the transistor to ensure that it operates in the active region.

(d) Power rating of a transistor : The power rating of a transistor *is the maximum power that a transistor can handle without damaging it.*

When a transistor is in operation, almost all the power is dissipated at the reverse biased collector-base junction. Thus, the power rating or maximum power dissipation is given by

$$\begin{aligned} P_D &= \text{Collector current} \times \text{Collector-base voltage} \\ &= i_c \times V_{cb} \\ &= i_c + \upsilon_{ce} \text{ as } V_{cb} \simeq V_{ce} \end{aligned}$$

In a transistor circuit, it should be ensured that its power rating is not exceeded, otherwise the transistor may be damaged due to excessive heat.

• 3.16. MERITS OF TRANSISTOR

Transistor have a number of advantages over electron valves—which are as follows :

(i) The transistors are robust, cheap and very small in size.

(ii) The transistors can operate with a small power supply (few volts).

(iii) When switched on, the transistors come into action immediately.

(iv) The transistors, being solid crystals are capable of bearing mechanical shocks.

(v) The transistors have a much larger life than valves.

Demerits : On account of a number of merits, the transistors have replaced the valves in electronic circuits. However, they suffer from one demeri that they are not suitable for large currents. They are likely to be destroyed when overheated.

• 3.17. BASE REGION OF A TRANSISTOR

The base region of a ransistor is made very thin to reduce the probability of the recombinaion of holes and electrons in this region. This probability is further reduced by using a lightly doped base. Most of the charge carriers coming from the emitter diffuse across the base (nearly 95%) and reach the collector. So the base current is very small and the collector current is nearly equal to the emitter current. This leads to large voltage and power gain.

If the base region were made thick, the base current would increase, thereby decreasing the collector current and defeating the very purpose of transistor.

• TEST YOURSELF

1. What are current gain α and β in common base and common emitter configuratin respectively.

---

2. Deduce the relation between α and β.

---

3. Define current amplification factor γ.

---

4. Deduce the relation between γ and α.

---

5. What is the importance of load line ?

• EXERCISE

1. What is bipolar junction transistor ? Distinguish between two types of transistors and explain their working.
2. What are he various configurations of transistor connections ? Discuss the important features of common base *p-n-p* transistor.
3. Discuss the characteristics of common emitter *p-n-p* transistor.
4. How will you draw d.c. load line on the output characteristics of a transistor ?
5. What is the meaning of transistor biasing ? What do you mean by Quiescent (Q) point and how is it selected ?

6. What are the essentials of a transistor biasing circuit ? Describe the various methods used for transistor biasing.
7. What do you understand by hybrid parameters ? What are their dimensions ? How will you measure h-parameters of a linear circuit ?
8. Derive the general formulae for input impedance, current gain and voltage gain in terms of h-parameters and the load.
9. How are h-parameters of a CE transistor amplifier measured experimentally ? Write the limitations of h-parameters.
10. The base of a transistor is
    (a) thin (b) thick (c) very thick (d) None of the above
11. The base of a transistor is doped :
    (a) heavily (b) lightly (c) both the above (d) None of the above
12. The relation between emitter current base current, and collector current is
    (a) Emiter current = Base current + Collector current
    (b) Collector current = Emitter current base current
    (c) Base current = Emitter current + Collector current
    (d) None of the above
13. The universally used transistor circuit configuration is :
    (a) Common collector (b) Common emitter
    (c) Both the above (d) None of the above
14. The input resistance of a transistor with respect to output resistance is always :
    (a) greater (b) equal (c) less (d) none of the above
15. Current gain α in common base configuration is given by :
    (a) $\alpha = \frac{i_e}{i_c}$ (b) $\alpha = \frac{1}{1 - i_e}$ (c) $\alpha = \frac{i_c}{i_e}$ (d) $\alpha = \frac{i_c}{1 - i_e}$
16. The relation between α and β is :
    (a) $\beta = \frac{1 - \alpha}{\alpha}$ (b) $\beta = \frac{1 + \alpha}{\alpha}$ (c) $\beta = \frac{\alpha}{1 + \alpha}$ (d) $\beta = \frac{\alpha}{1 - \alpha}$

• ANSWERS

10. (a) **11.** (b) **12.** (a) **13.** (b) **14.** (c) **15.** (c) **16.** (d)

U N I T - IV

FIELD EFFECT TRANSISTORS (FET)

STRUCTURE

- Field Effect Transistor (FET)
- Construction of FET
- Drain Characteristics of FET
- Transfer Characteristics of JFET
- FET Parameters
- JFET
- MOSFET
- Modes of MOSFET
- Enhancement type MOSFET
- Operational Amplifier (OP-Amp)
- Inverting Operational Amplifier
- Inverting Summing OP-AMP
- Non-inverting OP Amplifier
  - Test yourself
  - Exercise
  - Answers

LEARNING OBJECTIVES

After learning this chapter, you will be able to know

- Study of field effect transistors (FET)
- Construction of FET.
- Drain and transfer characteristics of FET.
- FET parameters.
- Study of MOSFET.
- Types of MOSFET.
- Study of operational amplifiers (Inverting and non-inverting).

• 4.1. FIELD EFFECT TRANSISTOR (FET)

The ordinary or bipolar transistor has two main disadvantages. Firstly, it has a low input impedance and secondly it has a considerable noise-level. The field effect transistor (FET) has, by virtue of its construction and biasing, large input impedance and much less noisy than the ordinary or bipolar transistor.

"A field effect transistor is a three terminal semi-conductor device in which current is carried by one type of carriers i.e., electrons or holes and is controlled by the variation of an electric field".

Since the current through a FET is controlled by an electrostatic field, therefore, it is called a 'Field Effect Transistor' and as the operation depends only on the motion of one type of charge carriers, it is also called an **unipolar transistor.** There are two types of field effect transistor (a) the junction field effect transistor (JFET) and (b) the insulated gate field effect transistor (IGFET), which is also known as metal oxide semiconductor field effect transistor (MOSFET).

Difference between FET and BJT :

Following are the differences between field effect transistors and bipolar junction transistors.

(i) In a FET, there is only one type of carriers, holes or electrons (unipolar). In an ordinary transistor both holes and electrons play part in the conduction of current (bipolar).

(ii) The input circuit (gate to source) of a FET is reverse biased and so the device has high input impedance. However, the input circuit of an ordinary transistor is forward biased and hence has low input impedance.

(iii) The FET is a volage-driven device *i.e.*, the input voltage controls the output current. The ordinary transistor is a current operated device *i.e.*, the input current controls the output current.

(iv) The bipolar transistor gain is characterised by current gain whereas, the FET gain is characterised as a transconductance *i.e.*, the ratio of change in output current to the input voltage.

(v) In FET, there are no junctions as in an ordinary transistor. The conduction is through an *n*-type or *p*-type semi-conductor material.

Advantages of FET : (a) The FET has an extremely high input impedance of the order of 100 mega ohms.

(b) The FET has lower noise level than BJT and therefore, is more suitable for the input stages of low level amplifiers.

(c) The FET can be manufactured easily.

(d) The FET has no offset voltage such as base to emitter voltage in BJT to overcome. This property is very important in the applications like switch, chopper etc.

(e) The FET is immune to radiations.

(f) The FET shows better thermal stability. Therefore, it is not likely to be damaged by overheating.

(g) The FET draws very lower power in the digital circuits.

(h) The FET has a smaller size and longer life. Hence a larger number of them can be incorporated in integrated circuits.

Disadvantages of FET : (a) The FET shows poor performance at high frequency.

(b) The FET has small gain band-width in comparison to the BJT.

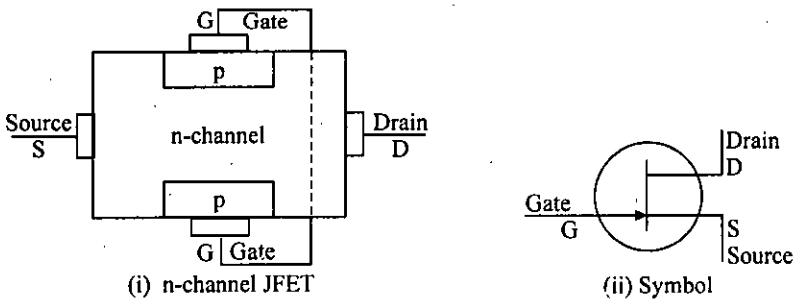
(c) The FET shows poor voltage gain.

(d) The FET can be operated only in low power applications.

• 4.2. CONSTRUCTION OF FET

The junction field effect transistors are classified into two classes (i) *n*-channel JFET and (ii) *p*-channel JFET.

(i) *n*-channel JFET : It consists of a *n*-type silicon bar containing two *p-n* junctions at the sides. The bar forms the conducting channel for the charge carriers which are electrons in this case. The two *p-n* junctions forming diodes are connected internally and a common terminal called **Gate** is taken out. Other terminals are source and drain taken out from the bar as shown in the Fig. 1 (i). Thus a JFET has three terminals, *viz.*, gate (*G*), source (*S*) and drain (*D*).



(i) n-channel JFET (ii) Symbol

Fig. 1

(ii) *p*-channel JFET : It consists of a *p*-type silicon bar containing two *p-n* junctions in the sides and *n*-type regions diffused on both sides. In this case the majority charge carriers are holes. Fig. 2 (i) shows the *p*-channel JFET and fig. 2 (ii) represents its symbol.

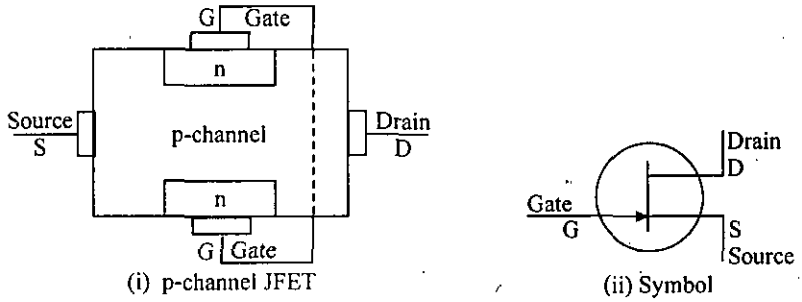


Fig. 2.

Working principle of FET (*n*-channel) : Fig. 3 shows the circuit of *n*-channel FET. The circuit action is as follows :

When a positive voltage V_{DS} is applied between drain and source terminals and voltage on the gate is zero, the two *p-n* junctions at the sides of the bar establish depletion layers. The electrons flow form source to drain through a channel between the depletion layers.

When a reverse voltage V_{GS} is applied between the gate and source, the width of the depletion layers is increased, thereby reducing the width of conducting channel and increasing the resistance of *n*-type bar. Therefore, the current from source to drain decreases. Similarly, if the reverse voltage on the gate is decreased, the current increases.

Obviously, the current from source to drain can be controlled by the application of potential (electric field) on the gates.

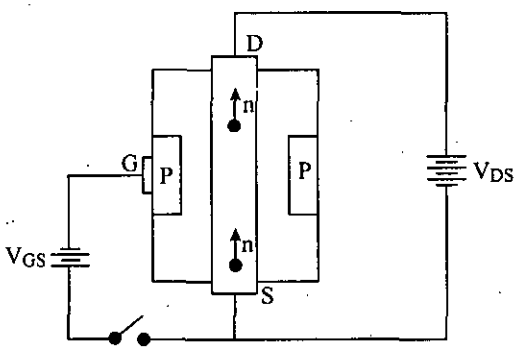


Fig. 3.

Working of FET (*p*-channel) : The working of a *p*-channel FET is similar to that of *n*-channel FET with the difference that the channel current carriers are holes instead of electrons and the polarities of the voltages V_{GS} and V_{DS} are reversed.

• 4.3. DRAIN CHARACTERISTICS OF FET

The curve between drain current I_D and drain-source voltage V_{DS} of a FET at constant gate-source volage (V_{GS}) is called drain characteristics or output characteristics of FET. Fig. (4) shows the circuit for determining the drain characteristics of a FET.

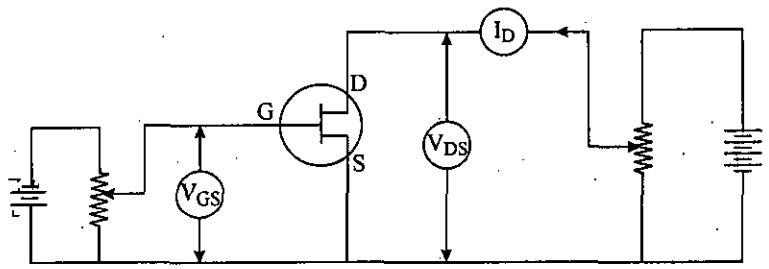


Fig. 4. Circuit for drain characteristics of a *n*-channel FET.

To draw the drain characteristics, V_{GS} is given a fixed value (say –1V) and V_{DS} is changed in steps and corresponding value of I_D current is noted. V_{GS} is given another fixed value and a set of observations of V_{DS} and I_D is noted. The procedure is repeated and plots of V_{DS} versus I_D are drawn for different fixed values of V_{GS}. The curves obtained are shown in the Fig. (5). In general each characteristics has three portions, a linear region, a saturation region and a breakdown region. The characteristics resemble that of a pentode valve. To explain the curves, let us suppose the gate source

voltage $V_{GS} = 0$ V and the drain source voltage V_{DS} is increased. This results in increasing the drain current I_D linearly. As a result the thickness of the depletion region also increases thus increasing the channel resistance. A condition is obtained when the two depletion regions met and the channel resistance prevents further rise in the drain current. This is called **'Pinch off'.** The values of the saturation current and voltage are called **pinch off current** I_{DSS} and the **pinch off voltage** V_P respectively. The further rise in V_{DS} breaks down the junctions and large current flows. If V_{GS} is increased (more negative) the pinch off condition is arrived at a lower value of drain current. Thus the gate potential acts as a control for drain current.

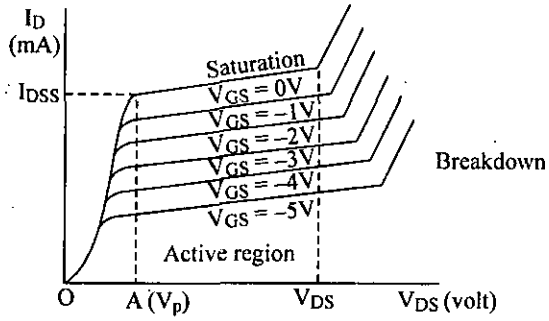


Fig. 5. Output characteristics of an *n*-channel JFET.

The following points are of importance :

(i) I_{DSS} is measured under shorted gate conditions : It is the maximum drain current that can be obtained with normal operations of JFET.

(ii) V_{DS} (max) is the maximum drain voltage that can be applied to a JET. If the drain voltage exceeds this value FET would break down.

(iii) The region between V_P and V_{DS} (max) is called **active region.** In this region the JFET behaves like a constant current source. For proper working, the JFET must be operated in this region.

• 4.4. TRANSFER CHARACTERISTICS OF JFET

The transfer characteristics is a curve beween the drain current and the gate-source voltage V_{GS} for a constant value of drain source voltage (V_{DS}). The method to obtain the curve is the same as discussed in 4.3. The curve is shown in the Fig. (6).

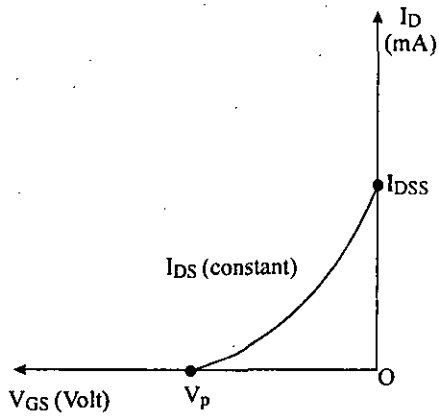


Fig. 6.

There are two important points in a transfer characteristic (i) Pinch off currents I_{DSS} when V_{GS} is zero and (ii) The pinch off voltage V_P ($I_D = 0$). It is the gate-source voltage where the channel is completely cut off and the drain current becomes zero. As the reverse gate-source voltage V_{GS} is increased, the cross sectional area of the channel decreases. This in turn decreases the drain current. At some value of V_{GS}, the depletion layer extend completely across the channel. In this condition, the channel is cut off and the drain current reduces to zero.

• 4.5. FET PARAMETERS

FET has cerain parameters which determine its performance in a circuit. The main parameters are (i) Drain resistance (ii) Transconductance (iii) Amplifications factor.

(i) Drain resistance : It is defined as **the ratio of the change in drain source voltage (ΔV_{DS}) to the corresponding change in drain current (ΔI_D) at constant gate-source voltage (V_{GS}).**

$$r_D = \left[\frac{\Delta V_{DS}}{\Delta I_D}\right]_{V_{GS} \text{ constant}}$$

The drain resistance has a large value ranging from 10 KΩ to 1 MΩ.

(ii) Transconductance : It is defined as **the ratio of the change in drain current (ΔI_D) to the change in gate-source voltage (ΔV_{GS}) at constant drain source voltage *i.e.,***

$$g_{fs} = \left[\frac{\Delta I_D}{\Delta V_{GS}}\right]_{V_{DS} \text{ constant}}$$

This is expressed in mA/volt or micro mhos. Its value ranges from 2 to 6 milli-mhos.

(iii) Amplification factor : It is defined as **the ratio of change in drain-source voltage (ΔV_{DS}) at constant drain current (I_D) *i.e.,***

$$\mu = -\left[\frac{\Delta V_{DS}}{\Delta V_{GS}}\right]_{I_D \text{ constant}}$$

The minus sign indicates that V_{DS} and V_{GS} must be of opposite sign in order to keep I_D as constant. The amplification factor signifies the effectiveness of the gate voltage over the drain voltage in controlling the drain current. Its value ranges from 50 to 150.

Relation among FET parameters : We have

$$\mu = \frac{\Delta V_{DS}}{\Delta V_{GS}}$$

$$= \frac{\Delta V_{DS}}{\Delta I_D} \times \frac{\Delta I_D}{\Delta V_{GS}} \text{ (multiplying and dividing by } \Delta I_D)$$

or $\mu = r_D \times g_{fs}$.

i.e., amplificatin factor = drain resistance × transconductance

• 4.6. JFET

A JFET has three terminals *viz.,* source, gate and drain. However four terminals are required for connection in a circuit two for the input and two for the output. So one terminal of JFET is made common to both input and output terminals and hence a JFET can be connected in the following three arrangements.

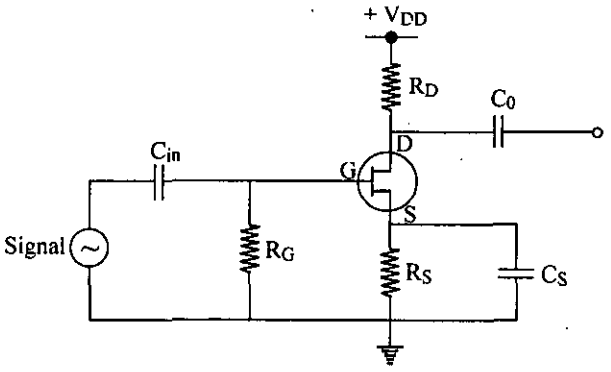


Fig. 7. Common source connections of a *n*-channel JFET amplifier.

(i) Common gate (ii) Common source (iii) Common drain.

Out of the above three, common source connection is the most commonly used. Fig. (7) shows this configuration.

Merits : This arrangement, has the following merits :

(i) The input impedance is high.

(ii) The voltage gain is good.

(iii) The output impedance is moderate.

Demerits : This circuit produces a phase reversal *i.e.,* the output signal is 180° out of phase with the input signal.

• 4.7. MOSFET

Another more useful class of FET is the metal oxide semiconductor field effect transistor.

In this FET, the channel resistance is controlled by an electric field owing to a capacitor unlike a *p-n* junctin in a JFET.

Construction : The construction of MOSFET is similar to that of FET with the following modifications :

(i) There is only a single *p*-region called **substrate.**

(ii) Metal gate is insulated by a very thin oxide layer from the semi-conductor channel. Therefore, it is also known as the **insulated gate field effect transistor** (IGFET). Figure (8) shows the constructional details and symbols of *n*-channel MOSFET.

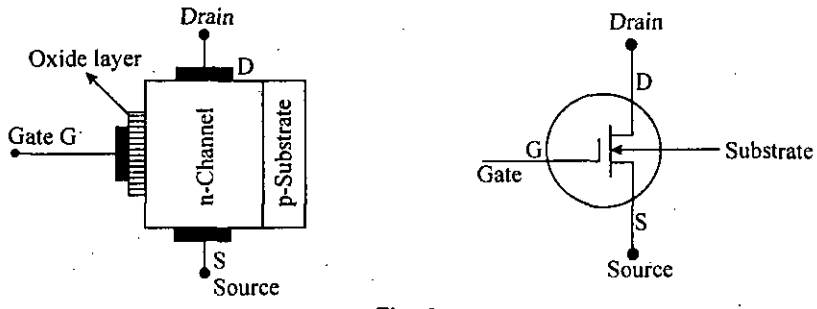


Fig. 8.

Working principle of MOSFET : *Fig. (9) shows the circuit diagram of a MOSFET.* The gate forms a small capacitor whose one plate is the gate and other plate is the channel with metal oxide in between them as the dielectric. When negative voltage is applied to the gate, electrostatic field is set up between the capacitor plates. Electrons accumulate at the gate and repel the conduction band electrons in the *n*-channel. Therefore, leser number of conduction electrons are available for the current conduction through the channel. This current from source to drain decrease, with increase in the negative voltage of the gate. If the gate is given positive voltages, this current increases.

Differences : (i) In JFET, the conductivity of the channel is controlled by an electric field across a *p-n* junction, whereas in MOSFET, it is controlled by the field of a parallel plate capacitor.

(ii) In MOSFET, due to gate capacitor, negligible gate current flows whether positive or negative voltage is applied at the gate. Therefore, the input impedance of MOSFET is very high (10^4 MΩ – 10^6 MΩ).

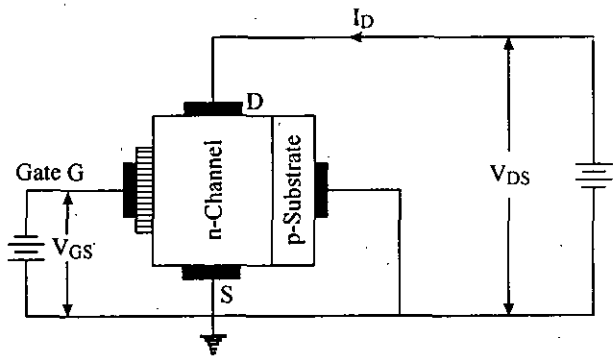


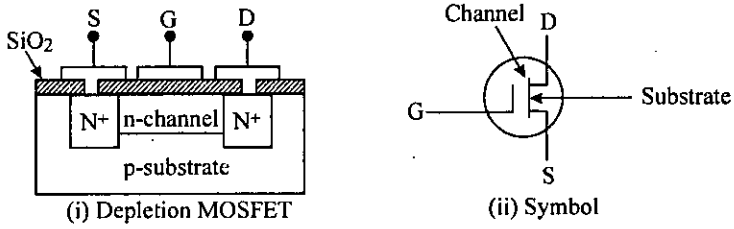
Fig. 9.

(iii) JFET can be operated in depletion mode only whereas MOSFET can be operated in depletion as well as in enhancement mode.

• 4.8. MODES OF MOSFET

There are basically two types of MOSFET. The first type in which the channel is physically constructed between the source and the drain, is known as **Depletion MOSFET.** The other type, in which no channel is constructed at the time of manufacturing but it is developed only when voltage is applied to the gate is known as **Enhancement MOSFET.** Each of the two types may be either *n*-channel MOSFET or *p*-channel MOSFET.

Depletion MOSFET : The *n*-channel MOSFET is formed on a *p*-substrate (*p*-doped semi-conductor). The source and the drain regions are formed by diffusing heavily doped *n*-type material (N^+) into the substrate. The regions are connected to the source and the drain terminals by metal ohmic contacts. An *n*-channel is diffused between the source and the drain onto the substrate. An insulating layer of Silicon dioxide (SiO_2) is deposited above the *n*-channel. A metallic layer is deposited above this (SiO_2) layer and is connected to the gate terminal. This metal layer functions as one plate of the capacitor, *i.e.,* SiO_2 acts as the dielectric and the *n*-channel semi-conductor material acts as the other plate of the capacitor. This gate capacitor makes the gate input impedance of a MOSFET very large. The substrate is internally connected to the source terminal. Fig. 10 (i) shows the constructional details of a Depletion MOSFET and Fig. 10 (ii) shows its symbol.



(i) Depletion MOSFET (ii) Symbol

Fig. 10.

Depletion MOSFET characteristics : Fig. 11 (i) shows the basic circuit diagram of *n*-channel depletion MOSFET. The substrate is internally connected to the source which is grounded. V_{DS} is the positive voltage between the drain and the source, V_{GS} is the negative voltage supplied to the gate between the gate and the source and I_D is the drain current. Fig. 11 (ii) shows the drain characteristic curves and Fig. 11 (iii) shows the transfer characteristics of *n*-channel depletion MOSFET. The negative gate-source voltage V_{GS} push electrons out of the channel to deplete it. On the other hand positive V_{GS} values result in an increase in the channel size as the *p*-type carriers are pushed away. This rsults in larger channel current. The drain current

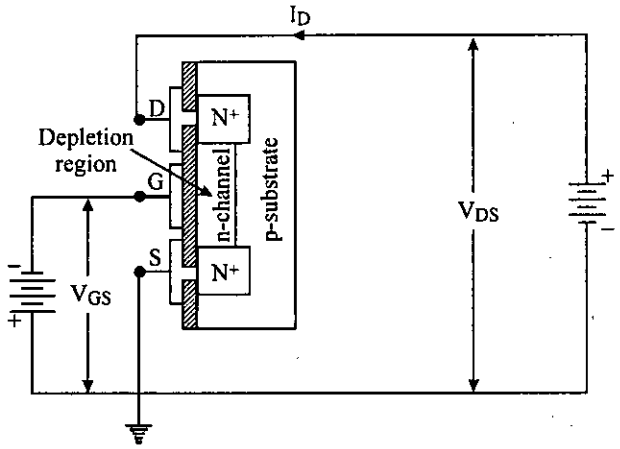


Fig. 11. (i)

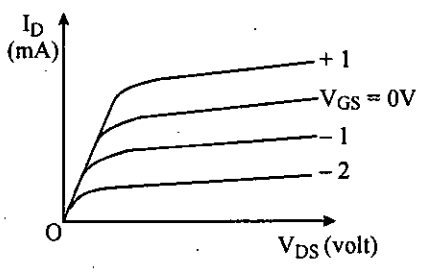


Fig. 11. (ii)

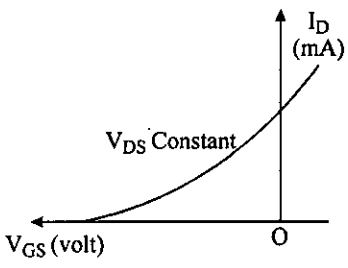


Fig. 11. (iii)

progressively decreases to almost zero as V_{GS} is made more and more negative. The characteristics curves are similar to those for JFET.

The transfer characteristics (plot of I_D versus V_{GS} for constant value of V_{DS}) continue for positive values of V_{GS} also. This MOSFET can be operated with either polarity of V_{GS} because the gate is isolated from the channel for both negative and positive values of V_{GS}.

• 4.9. ENHANCEMENT TYPE OF MOSFET

This constructional details of an enhancement type MOSFET is the same as that of depletion type with the difference that in the case of an enhancement MOSFET, no channel is diffused as shown in the Fig. 12 (i). The Fig. 12 (ii) shows the symbol of he type of MOSFET. No channel is shown by he broken line.

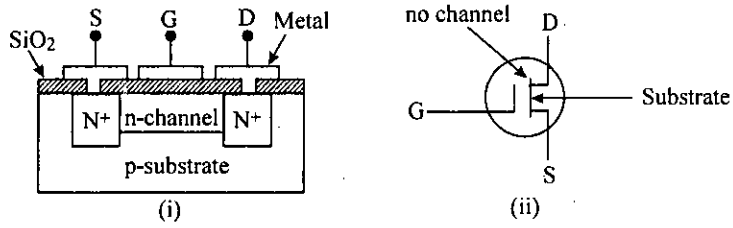


Fig. 12.

Enhancement MOSFET characteristics : The Fig. 13 (i) shows the drain characteristics (output curves) and figure 13 (ii) shows the transfer characterisics of an enhanced MOSFET.

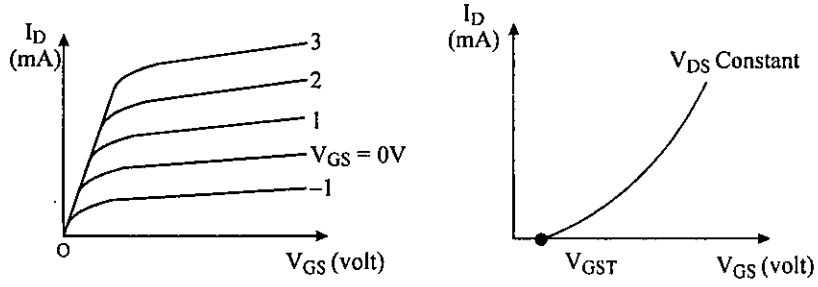


Fig. 13. Output characteristics, (ii) Transfer characteristics.

In enhanced MOSFET, there is no channl between the source and the drain. When a positive V_{GS} is applied, the holes are repelled from the p-substrate under the gate region and thus this region is depleted with further increase in V_{GS}, the electrons are attracted into the depletion region making it like a n-channel between the source and the drain. For smaller values of V_{GS}, there is no drain current. It is available only when V_{GS} is sufficient enough to create a channel. The drain current grows first slowly and then repidly. The minimum voltage of he gate which starts the drain current is called **'gate-source threshold voltage'** V_{GST} shown in Fig. 13 (iii). Since the drain current is 'enhanced' by the positive gate voltage, this MOSFET is called an **'Enhancement type'.**

• 4.10. OPERATIONAL AMPLIFIER (OP-AMP)

The operational amplifier basically consists of a very high gain d.c. amplifier with feedback, having high input impedance, low ouput impedance and acting as a differential amplifier. The operational amplifiers were originally used to perform mathematical functions such as addition, integration, differentiation etc. in analogue computers. Now they are also used as comparator, pulse generator and square wave generator etc. Presently the operational amplifier employs integrated technology and are widely used.

Ideal operational amplifier : An ideal OP-Amp is one which has an infinitely high value of voltage gain and an infinite input impedance. However, these values associated with practical amplifiers are not infinite but are very high.

An ideal operational amplifier has the following characteristics :

(i) Input impedance $Z_i = \infty$ (ii) Output impedance $Z_0 = 0$

(ii) Voltage gain $A = -\infty$ (iv) Band width $BW = \infty$

The characteristics do not drift with temperature. The ideal OP-amp is shown in the Fig. 14 (i) and its low frequency equivalent in Fig. 14 (ii). A signal appearing at the negative terminal 1 is inverted at the output and is called **inverting terminal** while a signal at the positive terminal 2 appears at the output without any change in sign and is called **non-inverting terminal**. In general, the output voltage is directly proportional to the input voltage which is difference of V_1 and V_2 *i.e.*, $V_i = V_2 - V_1$ and $(-A)$ is the voltage gain of the amplifier.

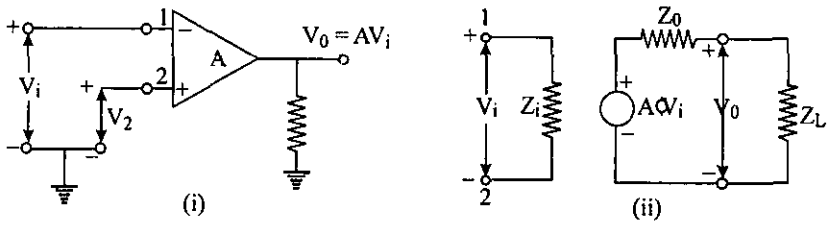


Fig. 14.

OP-Amp. parameters : The OP-AMP are widely used in d.c. or a.c. amplifiers. In d.c. amplifier applications, the output voltage may have an added error component. In order to minimise this error, certain OP-AMP characteristics which are responsible for the error, are (i) input bias current (ii) input offset current, (iii) input offset voltage and (iv) drift etc.

In a.c. amplifier applications, the OP-AMP characteristics that are to be considered are frequency response and slew rate.

(1) Input bias current : The output of an ideal OP-AMP is zero when the two input are identical *i.e.*, $V_0 = 0$ if $V_1 = V_2$. However due to mismatch of the input transistors, different bias currents flow through the input terminals. The **Input bias current** is the current flowing into each of the two input terminals when they are biased to the same voltage levels or the average of the currents into the two input terminals with output at zero volt ($V_0 = 0$, Fig. 15).

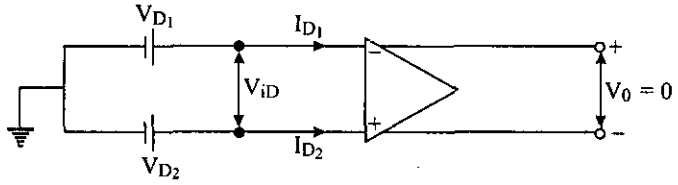


Fig. 15.

$$I_{\text{bias}} = \frac{I_{D_1} + I_{D_2}}{2}$$

(2) Input offset current : The input offset current I_{i_0} is defined as the difference of the currents into the two input terminals with the output at zero volt.

$$I_{i_0} = I_{D_1} - I_{D_2} \text{ with } V_0 = 0$$

(3) Input offset voltage : This is defined as the input voltage applied across the input terminals to have zero output voltage.

However in practice, the output voltage is not zero, even if equal voltage are applied to the input terminals. To obtain this input offset voltage V_{i_0} of the order of 1–4 mV is

required. This value drifts with change in temperature. If ΔV_{i_0} is the drift in input offset voltage corresponding to a change ΔT in temperature, the **drift** is defined by $\frac{\Delta V_{i_0}}{\Delta T}$.

(4) Input common mode range : It is the maximum differential signal that can be applied safely to OP-Amp inputs.

(5) Output offset voltage : It is the difference between the d.c. voltages at the two output terminals.

(6) Power supply voltage rejection ratio : It is defined as input offset voltage change per unit supply voltage change.

(7) Output voltage swing (range) : This is a function of the supply voltage and is the maximum peak to peak output voltage which can be obtained without any distortion in the waveform.

(8) Full power bandwidth : It is the maximum frequency over which the complete output swing can be obtained.

(9) Slew rate : This is defined as the maximum rate of change of output voltage for a step input.

$$\text{Slew rate } S = \left[\frac{dV_0}{dt}\right]_{\max}$$

• 4.11. INVERTING OPERATIONAL AMPLIFIER

Fig. 16 (i) below shows the inverting OP-AMP and fig. 16 (ii) its equivalnt circuit. The positive input of the amplifier is grounded and the input signal is applied to the negative input signal of the amplifier through impedance Z_1. The feedback applied through the impedance Z_2 from the output to the input is negative.

If the OP-AMP is considered as ideal, it must have an infinite voltage gain. The gain A is defined as :

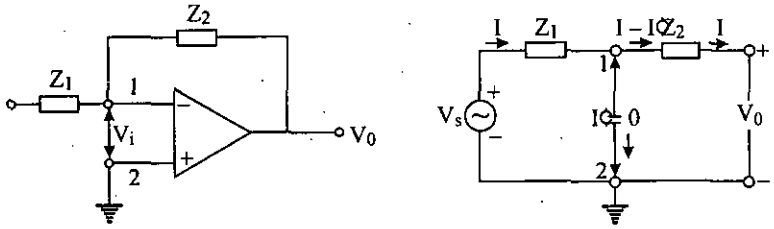


Fig. 16.

$$|A| = \frac{V_0}{V_i} \qquad ...(1)$$

For A to be infinite, $V_i \to 0$ *i.e.*, there is no potential difference between terminals 1 and 2 and so the current $I' = 0$. Thus the same current I flows though the impedances Z_1 and Z_2.

Current through Z_1 = current through Z_2

$$\therefore \quad \frac{V_s - V_i}{Z_1} = \frac{V_i - V_0}{Z_2}$$

$$\frac{V_0}{Z_2} = \frac{V_i}{Z_2} + \frac{V_i}{Z_1} - \frac{V_s}{Z_1}$$

$$= V_i\left[\frac{1}{Z_2} + \frac{1}{Z_1}\right] - \frac{V_s}{Z_1} \qquad ...(2)$$

Putting the value of V_i from eqn. (1), $\left[V_i = -\frac{V_0}{A}\right]$

$$\frac{V_0}{Z_2} = -\frac{V_0}{A}\left[\frac{1}{Z_2} + \frac{1}{Z_1}\right] - \frac{V_s}{Z_1}$$

or $$V_0\left[\frac{1}{Z_2} + \frac{1}{A}\left(\frac{1}{Z_2} + \frac{1}{Z_1}\right)\right] = \frac{V_s}{Z_1}$$

or $$\frac{V_0}{V_S} = -\frac{Z_2}{Z_1}\left[\frac{1}{1 + \frac{1}{A}\left(1 + \frac{Z_2}{Z_1}\right)}\right] \quad ...(3)$$

where $\frac{V_0}{V_s} = A_f$ is called the **closed loop gain** (with feedback) whereas A is called **open loop gain** (without feedback).

For ideal inverting OP-AMP, $V_i \to 0$, so from eqn. (2),

$$\therefore \quad \frac{V_0}{Z_2} = -\frac{V_s}{Z_1} \quad \text{or} \quad \frac{V_0}{V_s} = -\frac{Z_2}{Z_1} \quad ...(4)$$

The negative sign shows that the amplifier reverses the sign of the input voltage *i.e.*, the output is 180° out of phase with the input.

Features of an ideal inverting OP-AMP : (i) Input impedance $Z_i = Z_1$ (external impedance).

(ii) Output impedance $Z_0 = 0$.

(iii) Current in to each input terminals of the amplifier is zero.

(iv) Potential difference between input terminals is zero.

Practical inverting OP-AMP : Let us consider an amplifier which does not satisfy the above conditions of an ideal OP-AMP. So $A \neq \infty$, $Z_i \neq \infty$ and $Z_0 \neq 0$.

The practical OP-AMP is shown in the Fig. 17.

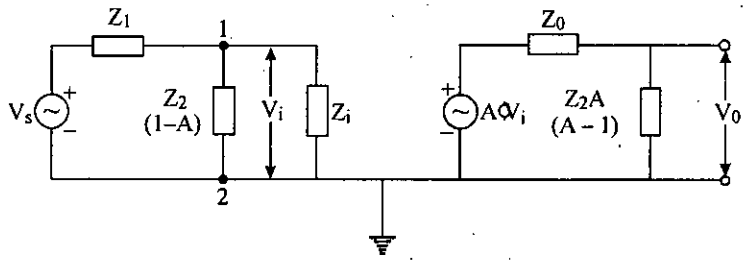


Fig. 17.

Z_2 is not shown in the figure as it has been accounted. A' is open circuit (or unloaded) voltage gain. Using Miller's Theorem, effect of feedback impedance Z_2 on the input and output of the amplifier is accounted by replacing it by two impedance *viz.*, $\frac{Z_2}{(1-A)}$ across the input and $\frac{Z_2 A}{(A-1)}$ across the output.

It can be shown that for such a circuit

$$\frac{V_0}{V_S} = \frac{-Z_2 / Z_1}{\frac{1}{A}\left(1 + \frac{Z_2}{Z_1} + \frac{Z_2}{Z_i}\right) - 1}$$

and $$A = \frac{V_0}{V_i} = \frac{A' + Z_0 / Z_2}{1 + Z_0 / Z_2}$$

If $Z_0 = 0$, then $A' = A$ so if $|A'| \to \infty$, then $|A| \to \infty$. So from eq. (3)

$$\frac{V_0}{V_s} = -\frac{Z_2}{Z_1}$$

Thus for high gain OP-AMP, the output voltage V_0 depends on the ratio $\frac{Z_2}{Z_1}$. Thus the feedback impedance Z_2 and input impedance Z_1 determine the precision of the operation to which the amplifier.

• 4.12. INVERTING SUMMING OP-AMP

It is the same as inverting amplifier with the difference that it has several input terminals. A simple amplifier circuit which adds several signals together is shown in the Fig. 18 below :

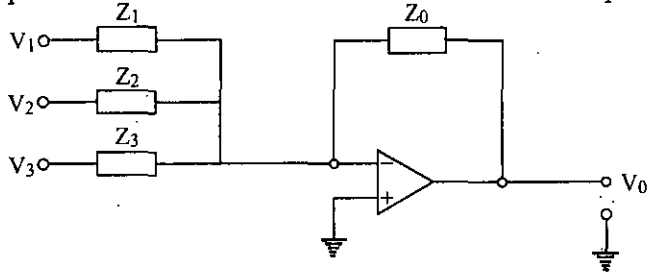


Fig. 18.

Virtual ground exists at the inverting terminal due to feedback and the input current to the ideal amplifier (As $Z_i = \infty$) is zero. Thus the current equation for the node at the inverting terminal is

$$\frac{V_1}{Z_1} + \frac{V_2}{Z_2} + ... \frac{V_n}{Z_n} + \frac{V_0}{Z_0} = 0$$

or
$$V_0 = -\left[\frac{Z_0}{Z_1} V_1 + \frac{Z_0}{Z_2} V_2 + ... \frac{Z_0}{Z_n} V_n\right]$$

Thus the output voltage is equal to the negative weighed sum of the input voltages.

If $Z_1 = Z_2 = ... Z$, then the output voltage is

$$V_0 = -\frac{Z_0}{Z}(V_1 + V_2 + ... V_n)$$

The output voltage is proportional to the sum of input voltages. Thus the circuit behaves as a summing amplifier. This type of amplifier may be used, for example, in an audio mixer unit which mixes signals from three or more signal sources.

• 4.13. NON-INVERTING OP-AMPLIFIER

In non-inverting OP-AMP the output is equal to and in phase with the input voltage. The Fig. 19 shows the circuit diagram for such an amplifier. Here the source and the load are effectively isolated *i.e.*, $Z_i = \infty$ and $Z_0 = 0$. As the input impedance is infinite, no current flows into either input terminals of the OP-AMP.

That is $I_1 = 0$ and $I_2 = 0$. The input signal V_s is applied directly to the non-inverting terminal 2. So no phase inversion takes place at the output. Some of the output is feedback to the inverting input providing effectively some voltage V_1 at the inverting terminal of the same polarity as at the non-inverting input.

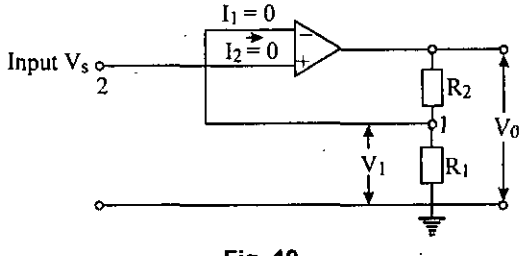


Fig. 19.

It is obvious from the figure that

$$V_0 = A(V_1 - V_s)$$

As $A = -\infty$, and V_0 is finite

$$\therefore \quad V_1 - V_s = 0 \quad \text{or} \quad V_1 = V_s$$

Then, the input voltage $V_i = V_1 - V_s$ is zero. As the current into the input terminal $I_1 = 0$, so the same current I flows through R_1 and R_2. From the Fig. 19, we have

$$V_1 = R_1\left(\frac{V_0}{R_1 + R_2}\right)$$

or $$V_s = R_1\left(\frac{V_0}{R_1 + R_2}\right)$$

or $$\frac{V_0}{V_s} = \frac{R_1 + R_2}{R_1}$$

$$= 1 + \frac{R_2}{R_1}$$

Thus the output depends on the ratio $\frac{R_2}{R_1}$. If $R_1 = \infty$, $V_0 = V_s$ that is the output voltage follows the input voltage. The OP-AMP in this case acts as a voltage follower.

Features of non-inverting OP-AMP : (i) No current flows into either input terminals.

(ii) The voltage at the two input terminals to the amplifier are equal ($V_1 = V_s$).

(iii) There is effectively no voltage drop at the input terminals as V_1 follows V_s. It means that effectively an open circuit results between input terminals.

• TEST YOURSELF

1. What is the difference between ρ-channel FET and *n*-channel FET.

.....

.....

2. Give 3 major differnce between JFET and MOSFET.

.....

.....

3. What do you understand by Transconductance. How does it effect the train resistance of JFET ?

.....

.....

4. Which transistor should be used at the input stage of the low level amplifier ? and Why ?

.....

.....

5. How is the working of an inverting summing or-any suitable for a device which mixes signals from three or more sources ? Explain ?

.....

.....

• EXERCISE

1. What are field effect transistors (FET) ? What is the difference between FET and a bipolar transistor ? Write the advantages and disadvantages of FET.
2. Describe the construction and working of a FET.
3. How will you determine the drain characteristics of FET ?
4. Draw and explain the transfer characteristics of JFET.
5. Define various FET parameters and find a relation among them.
6. What is MOSFET ? Give its construction and working principle. How does it differ from FET ?
7. Explain the models of MOSFET. Describe a depletion mode MOSFET and draw its characteristics.
8. Describe an enhancement mode of *n*-channel MOSFET. Draw and explain its characteristics.
9. What is an operational amplifier (OP-Amp) ? Explain the circuit diagram and its equivalent for the ideal OP-Amp. Mention various OP-Amp parameters.
10. Explain the circuit diagram of an inverting operational amplifier.

11. Explain the use of inverting OP-Amp as summing OP-Amp.
12. What is a non-inverting OP-Amp ? Draw and explain its circuit diagram.
13. JFET has the terminals :
    (a) 2 (b) 3 (c) 4 (d) none of the above
14. JFET is a transistor :
    (a) unipolar (b) bipolar (c) tripolar (d) none of the above
15. Voltage gain of FET with respect to ordinary transistor is :
    (a) less (b) equal (c) more (d) none of the above
16. Drain resistance of FET is :
    (a) $V_D = \left(\frac{\Delta V_{GS}}{\Delta I_D}\right)_{V_{DS}\text{ constant}}$ (b) $V_D = \left(\frac{\Delta I_D}{\Delta V_{GS}}\right)_{V_{DS}\text{ constant}}$
    (c) $V_D = \left(\frac{\Delta I_D}{\Delta V_{DS}}\right)_{V_{GS}\text{ constant}}$ (d) $V_D = \left(\frac{\Delta V_{DS}}{\Delta I_D}\right)_{V_{GS}\text{ constant}}$

• ANSWERS

13. (b) **14.** (a) **15.** (a) **16.** (d)

U N I T - V

SMALL SIGNAL AMPLIFIERS

STRUCTURE

LEARNING OBJECTIVES

After learning this chapter, you will be able to know

- Study of single stage amplifiers.
- D.C. and A.C. equivalent circuits of transistor amplifiers.
- Voltage and power gains in amplifiers.
- Classification of transistor amplifiers.
- RC coupled common emitter amplifier.
- Transformer coupled amplifier.
- Common source field effect transistor.
- Common drain field effect transistor.
- Study of feed back in amplifiers.

• 5.1. AMPLIFIER

An **amplifier** is the most important circuit of electronics. It strengthens or amplifies weak signal. Almost all electronic equipments include means for amplifying electric signals. The function of an amplifier is to accept very small signals at its input and amplify them to be used to perform some given function.

Single stage transistor amplifier

A single stage transistor amplifier is one which employees only one transistor with associated circuitory used for amplifying a weak signal.

A single stage transistor has one transistor, bias circuit and other axiliary components.

Practical circuits of transistor amplifier

The figure shows a practical single stage transistor amplifier. Here the transistor is usd in *CE* (common emitter) configuration. The various circuit element and their functions are described below :

(i) Biasing circuit : The resistances R_1, R_2 and R_E are elements of the biasing and stabilisation circuit. The values of the elements are fixed so as to establish a proper operating point, otherwise the output may not be obtained completely.

(ii) Input capacitance, C_{in} : A capacitor of the order of 10 μF is used to couple the signal to the base of the transistor. Otherwise the signal source resistance will form a parallel combination with R_2 and thus change the bias. The capacitor C_{in} will allow only a.c. signal to flow.

(iii) Emitter by-pass capacitor C_E : An emitter by-pass capacitor C_E of the order of 100 μF is used in parallel with R_E to provide a low reactance path to the amplified output, otherwise there will be voltage drop across R_E and the output voltage will be reduced.

(iv) Coupling capacitor C_c : One stage of amplification is coupled to the next stage by the coupling capacitor of the order of 10 μF, otherwise the bias conditions of the next stage will be changed due to the shunting effect of R_C. The coupling capacitor allows the flow of a.c. signal only of the first stage to the second stage.

Various circuit currents

The various currents in the amplifier circuit are shown in the Fig. 1. These are as follows :

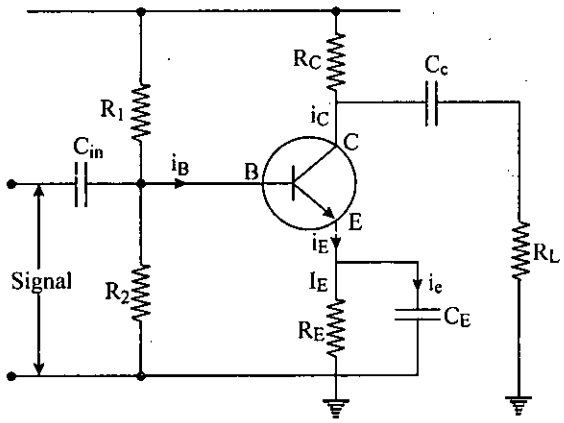


Fig. 1.

(a) Base current : In the absence of the signal, only the d.c. base current I_B flows due to biasing circuit. When a.c. signal is applied, a.c. base current i_b also flows. Thus, the total base current i_B is given by $i_B = I_B + I_b$.

(b) Collector current : In the absence of the signal, a d.c. collector current I_C flows due to the biasing circuit. When the a.c. signal is applied, a.c. collector current i_c also flows. Thus the total collector i_C is given by

$$i_C = I_C + I_c$$

where $I_C = \beta I_B$ = zero signal collector current

$i_c = \beta i_b$ = collector current due to signal

and β is current gain factor

(c) Emitter current : The total emitter current i_E with the application of signal is given by $i_E = I_E + I_e$

where $I_E = I_B + I_C$ = zero signal emitter current

and $i_e = i_b + i_c$ = emitter current with the application of signal

We know that the base current is usually very small, so to the approximation

$$I_E \simeq I_C \quad \text{and} \quad i_e \simeq i_c$$

• 5.2. D.C. AND A.C. EQUIVALENT CIRCUITS

Both d.c. and a.c. conditions prevail in a transistor amplifier circuit. The d.c. sources set up d.c. voltages and currents whereas the a.c. source (signal) produces a.c. voltages and currents. Therefore, the analysis of the action of a transistor is divided into two parts *viz.*, a d.c. analysis and an a.c. analysis. In the d.c. analysis, we consider all the d.c. sources and work out the d.c. voltages and currents in the circuit. In the a.c. analysis, we

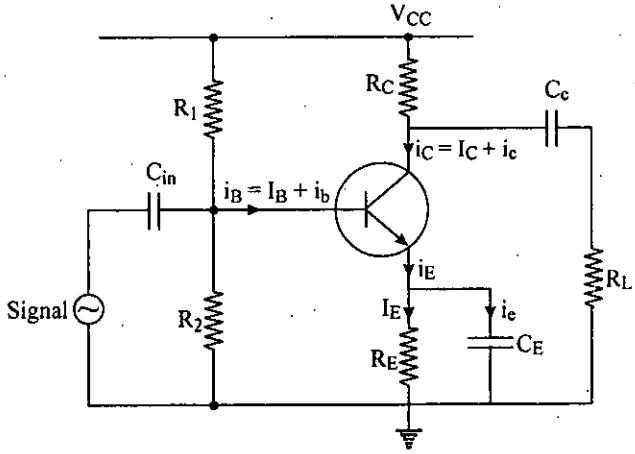


Fig. 2. Transistor amplifier circuit.

consider all the a.c. sources and work out the a.c. voltages and currents. The total currents and voltages are obtained by adding the d.c. and a.c. currents and voltages. Let us consider the following transistor amplifier circuit which is to be analysed by splitting it into d.c. equivalent circuit and a.c. equivalent circuit.

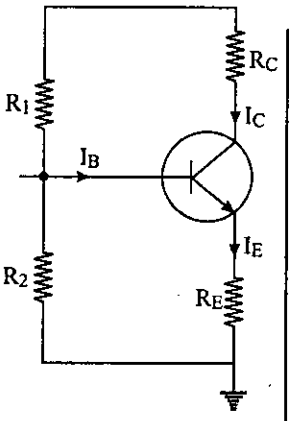


Fig. 3. d.c. equivalent circuit

(a) d.c. equivalent circuit : In the d.c. equivalent circuit of a transistor amplifier, only d.c. conditions are to be considered. Since the d.c. can not flow through a capacitor, all the capacitors look like open circuits in the d.c. equivalent circuit. The following two steps are applied in drawing the d.c. equivalent circuit.

(i) All the a.c. sourcs are deleted.

(ii) All the capacitors are removed or opened.

Accordingly, the d.c. equivalent circuit of the transistor amplifier shown above in the Fig. 2 is shown in Fig. 3.

(b) a.c. equivalent circuit : In the a.c. equivalent circuit of a transistor amplifier, only a.c. conditions are to be cosidered. The d.c. voltages is considered as zero. The capacitors are generally used to couple or by-pass the a.c. signal. Therefore, in order to draw the a.c. equivalent circuit, the following two steps are applied.

(i) All the d.c. sources are considered as zero.

(ii) All the capacitors are shorted.

Taking into considerations, the above two steps, the a.c. equivalent circuit of the transistor amplifier circuit shown in the Fig. 2 is shown in Fig. 4.

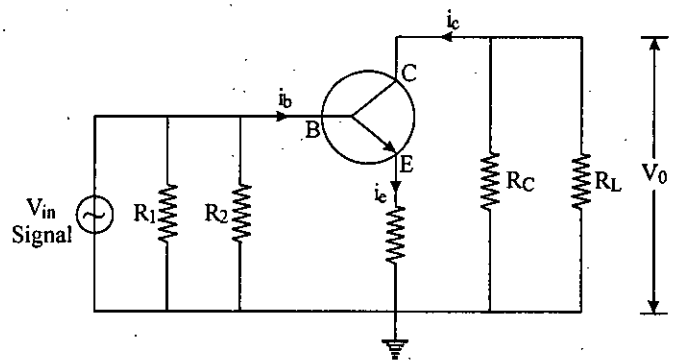


Fig. 4. a.c. equivalent circuit.

Voltage gain : The voltage gain of the transistor amplifier is defined as the **ratio of a.c. output voltage to the a.c. signal voltage.** It is clear from the Fig. 4, that the loads R_C and R_L are in parallel with each other. Therefore, the effective load for a.c. is given by

$$R_{AC} = \frac{R_C \times R_L}{R_C + R_L}$$

Now output voltage $V_0 = i_c \times R_{AC}$

Input voltage $V_{in} = i_b \times R_{in}$

$$\therefore \quad \text{Voltage gain } A_v = \frac{V_0}{V_{in}} = \frac{i_c \times R_{AC}}{i_b \times R_{in}}$$

$$= \beta \times \frac{R_{AC}}{R_{in}} \qquad \left(\because \beta = \frac{i_c}{i_b}\right)$$

$$\text{Power gain } A_P = \frac{i_c^2 R_{AC}}{i_b^2 R_{in}}$$

$$= \beta^2 \times \frac{R_{AC}}{R_{in}}$$

$$= \beta \times A_v$$

= current gain × voltage

• 5.3. PHASE REVERSAL IN A SINGLE STAGE COMMON EMITTER TRANSISTOR AMPLIFIER

When a.c. signal is applied at the input of a single stage emitter transistor amplifier, the output voltage is 180° out of phase with the applied input voltage. It means that when the input voltage increases in the positive direction, the output voltage increases in the negative direction and vice-versa. This is called **Phase reversal.**

The phase difference of 180° between the input signal voltage and the output voltage in a common emitter transistor amplifier is known as **phase reversal.** Fig. (5) shows the circuit diagram of a single common emitter transistor amplifier along with its input and output voltage waveform.

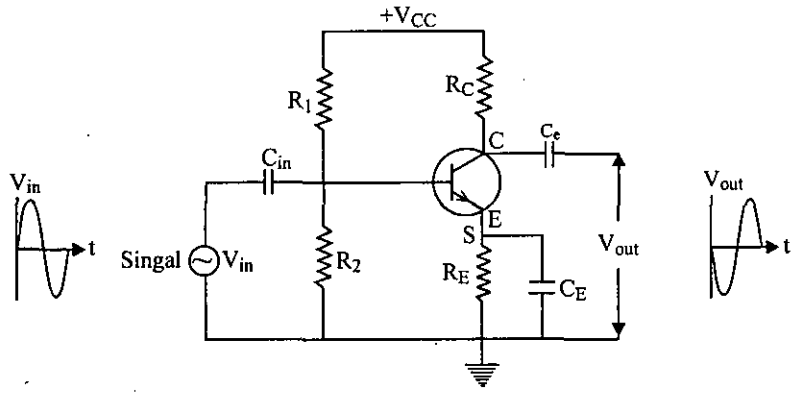


Fig. 5.

The signal to be amplified is applied at the input terminals between the base and the emitter. The output is derived from the collector and the emitter end.

The capacitor C_c is of the order of 10 μF which is negligible at ordinary signal frequencies. Therefore, it can be considered a short for the signal and the total instantaneous output voltage V_{CE} is given by

$$V_{CE} = V_{CC} - i_C R_C$$

Differentiating, we get

$$dV_{CE} = dV_{CC} - di_C R_C$$

Since V_{CC} is constant, $dV_{CC} = 0$

$$\therefore \quad dV_{CE} = -di_C R_C$$

The negative sign shows that the variation of output voltage is opposite to that of input voltage that is the output voltage is 180° out of phase with the input signal voltage.

• 5.4. CLASSIFICATION OF TRANSISTOR AMPLIFIERS

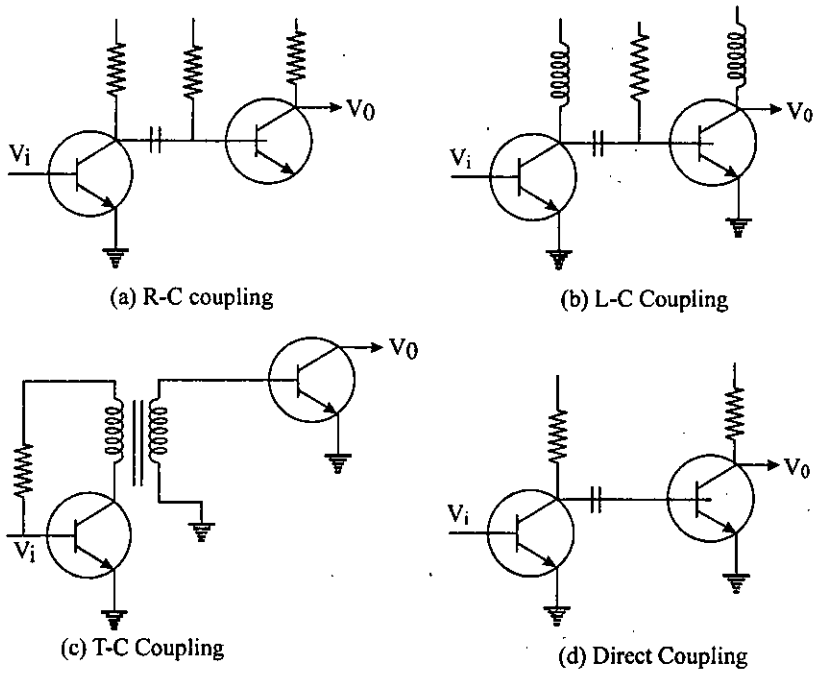
The transistor amplifiers may be classified according to their usage, frequency capabilities, method of coupling and mode of their operation.

(a) According to use : According to the usage, the amplifiers are classified as voltage amplifiers and power amplifiers. If the amplifier is used to increase the voltage level of the signal, it is called **voltage amplifier,** whereas if it increases the power level of the signal, it is called **power amplifier.**

(b) According to frequency capabilities : The amplifiers are classified according to the frequency range to which they are used. **Audio amplifiers** are those are used to which amplify the signals in the audio frequency range *i.e.,* 20 Hz to 20 KHz. **Radio frequency amplifiers** are used to amplify signals of very high frequency (above 20 KHz).

(c) According to coupling methods : The amplification due to a single stage amplifier is usually not very high whereas in practice, more amplification is required.

So multi-stage amplifiers are used for the purpose. The output from on stage is fed to the next stage. This is called **coupling.** According to the coupling device used, the amplifiers are classified as ***R-C* coupled, *L-C* coupled, transformer coupled,** and **direct coupled amplifier.** Various couplings are shown in the figure 6.



(a) R-C coupling (b) L-C Coupling

(c) T-C Coupling (d) Direct Coupling

Fig. 6.

Multistage amplifiers may be divided into following two categories :

(i) Cascade amplifiers : In cascade amplifiers, each stage and coupling between different stages are identical.

(ii) Compound amplifiers : In compound amplifiers, each stage as well as the coupling device may be different.

(d) According to mode of operation : The amplifiers are also classified according to their mode of operation as **Class A, Class *AB*, Class *B*** and **Class *C* amplifiers.**

(i) **Class *A* amplifier** is one in which the mode of operation is such that the collector current flows for the whole input signal.

(ii) **Class *AB* amplifier** is one in which the mode of operation in such that the collector current flows for more than half cycle, but less than the full cycle of the input a.c. signal.

(iii) **Class *B* amplifier** is one in which the mode of operation is such that the collector current flows for half cycle of the input a.c. signal.

(iv) **Class *C* amplifier** is one in which the mode of operation is such that the collector current flows for less than half cycle of the input a.c. signal.

• 5.5. TWO STAGE R-C COUPLED CE AMPLIFIER

This is a very popular type of coupling, usually employed for voltage amplification. Fig. 7 shows two stage *R-C* coupled *CE* amplifier. In the circuit R_1, R_2, R_C and R_E are used to provide the self bias and stabilisation network for the transistor. C_c is the coupling capacitor which connects the output of the first stage to the base (input) of the second stage. It transmits only a.c. signal at the end of one stage to appear at the input of the next stage but blocks d.c. part of the signal. C_E is a bypass capacitor which provides a low reactance path to the signal and prevents loss of amplification due to negative feedback.

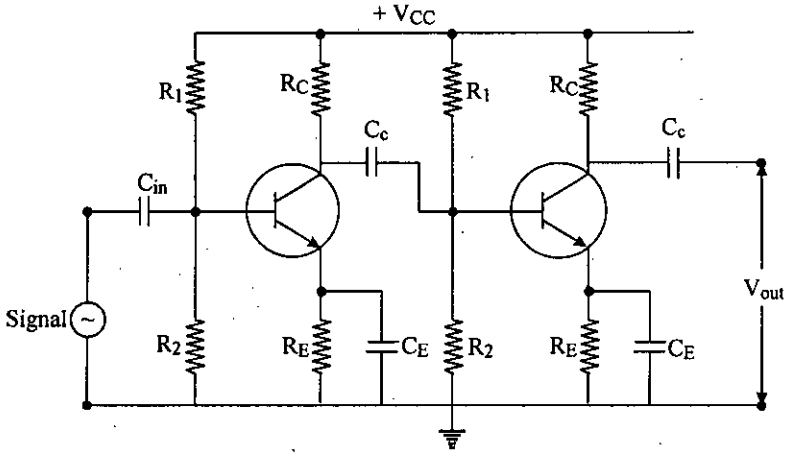


Fig. 7.

Operation : When a.c. signal is applied to the base of the first stage transistor, it is amplified. The amplified output which appears across R_C is given to the base of the second stage transistor through coupling capacitor C_c. This is further amplified by second stage and overall gain of the amplifier is considerably increased. The output is in phase with the input as it is reversed twice. It is to be noted that the total gain is less than the products of the gains of individual stages. The reason is that when a second stage is made to follow the first stage, the effective load resistance of the first stage is reduced due to the shunting effect of the input resistance of the second stage.

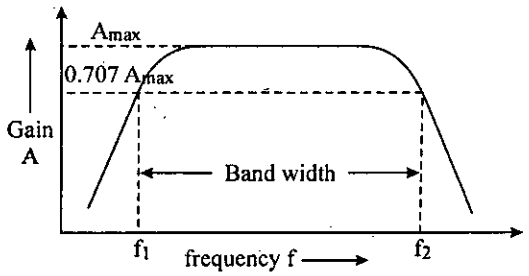


Fig. 8. Frequency response of R-C coupled amplifier.

Frequency response : The frequency response of an amplifier is a plot of voltage gain versus frequency. The frequency is plotted in logarithmic scale and the gain in decibles = 20 $\log_{10} A$. Figure 8 shows the frequency response curve which can be explained as below :

(a) At low frequencies : At low frequencies, the reactance of coupling capacitor C_c is very high and so a very small part of the signal passes from one stage to the next stage. Secondly the reactance of C_E is comparable to R_E and hence a.c. signal flows through the emitter R_E. This reduces the output voltage and also the gain at low frequencies.

(b) At high frequencies : The reactance of C_c at high frequencies is very small and it behaves as a short circuit. This increases the loading effect on the next stage and reduces the voltage gain.

(c) At middle frequencies : The voltage gain is constant in this frequency range. When frequency rises in this range, reactance of C_c decreases which tends to increase the gain. However at the same time, lower reactance means higher loading of the first stage and hence lower gain. These two factors almost cancel each other resulting in uniform gain at middle frequencies.

Band width : The band width of an amplifier is defined as the range of frequency over which the gain is equal to or greater than $\frac{1}{\sqrt{2}}$ or 70.7% of the maximum gain.

Band width = $f_2 - f_1$ = useful frequency range of operation.

Advantages : (i) It is inexpensive, as it employs resistors and capacitors which are cheap.

(ii) It is small, light and very compact as the modern parts are very small and light.

(iii) It has minimum possible non-linear distortion, as it does not use any coils or transformers which might pick up undesirable signals.

Disadvantages : (i) The gain of *R-C* coupled amplifier is comparatively small because of the loading effect to the next stage.

(ii) They have the tendency to become noisy is moist climate.

(iii) Impedance matching is poor as the output impedance is several hundred ohms while of a speaker is only few ohms.

• 5.6. CIRCUIT OF TWO STAGE R-C COUPLED CE AMPLIFIER

Fig. 9 shows a two stage *R-C* coupled amplifier which consists of two single stage transistor amplifiers using the CE configuration.

In the circuit R_1, R_2, R_c and R_e along with V_{CC} are used to provide the self-bias and stabilisation for the transistor. C_c is the coupling capacitor which connects the output of the first stage to the base of the second.

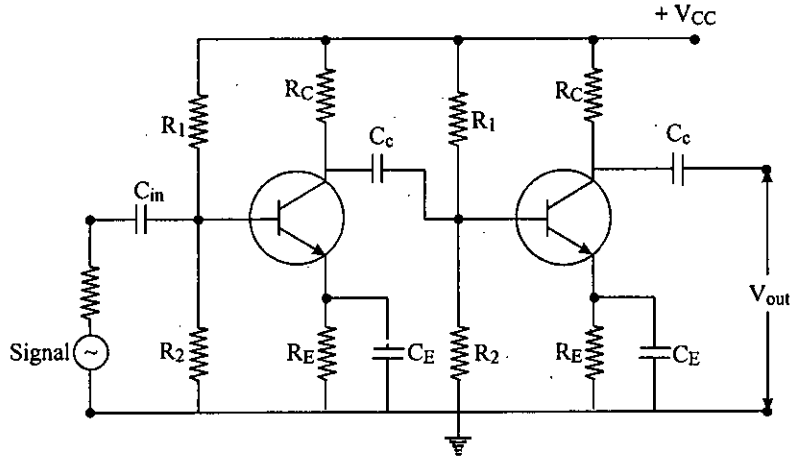


Fig. 9. Two stage R-C coupled amplifier.

Equivalent circuit : In order to draw the simplified equivalent circuit, following assumptions are made :

(i) The reverse voltage feedback may be neglected.

(ii) Output resistance is so large that it can be considered as an open circuit.

(iii) The reactance of C_e for any given input frequency is so small that the parallel combination of R_e and C_e can be effectively considered as a short circuit.

With the above assumptions, the simplified equivalent circuit is shown in the figure 10.

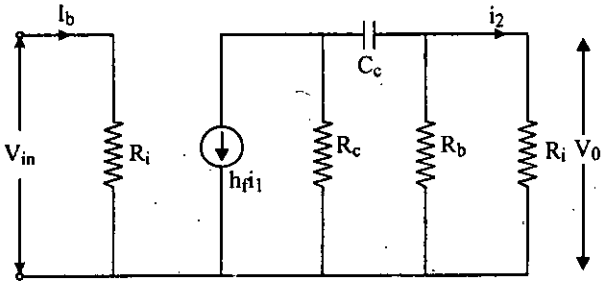


Fig. 10. Simplified equivalent circuit. (C_0 → The output capacitance of the first stage, input capacitance of next stage and stray and wiring capacitances)

For analysis purpose, the entire frequency range is divided into the following three frequency ranges.

Low frequency range : In the low frequency range, the impedance offered by coupling capacitor is comparable to the load resistance, so that the coupling capacity

largely affects the current amplification. Therefore, we have to include the capacity in the equivalent circuit. On the otherhand, the impedance offered by the shunting capacitor is so large as to behave an open circuit. Having these considerations, the equivalent circuit is shown in figure 11.

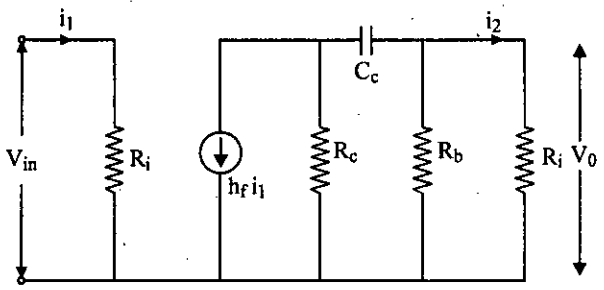


Fig. 11. (a) Equivalent circuit with current source (h_f → forward current ratio factor)

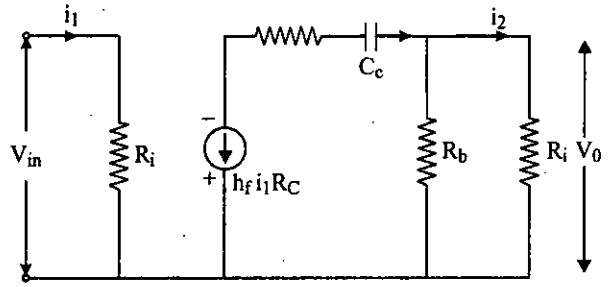


Fig. 11. (b) Equivalent circuit with voltage source.

Middle frequency range : At the middle frequency range, the impedance offered by C_c is so small as to be an effective short circuit while the impedance offered by shunting capacitor is comparatively so large as to behave an effective open circuit. Therefore, both can be eliminiated in this range of frequency. The simplified equivalent circuit at the middle frequency range is shown in the figure 12.

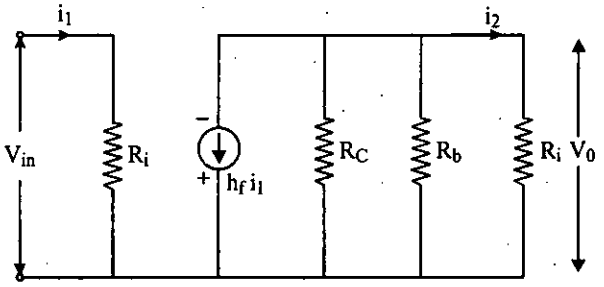
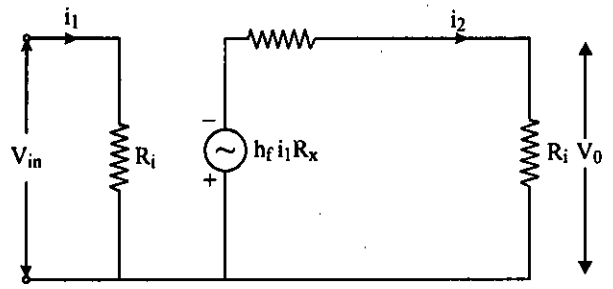


Fig. 12. (a) Equivalent circuit with current source.



$$R_x = \frac{R_b R_c}{R_b + R_c}$$

h_t → forward currentration factor

Fig. 12. (b) Equivalent circuit with voltage source.

High frequency range : In the high frequency range, the reactance offered by C_c is very small and so can be considered as short circuit. The reactance of C_0 will not be very large and so can not be considered as open circuit. With these considerations, the equivalent circuit is shown in the figure 13.

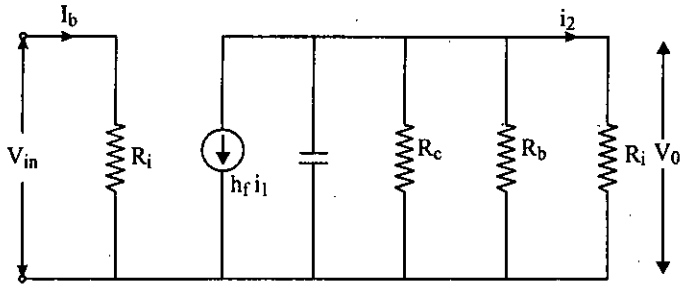


Fig. 13. (a) Equivalent circuit with current source.

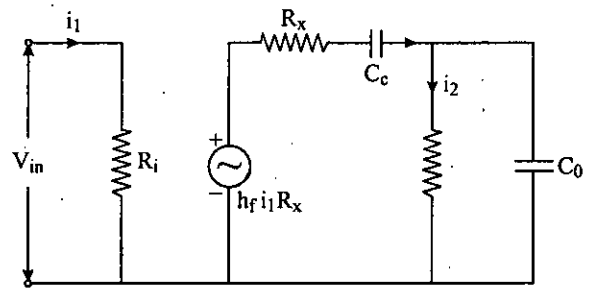


Fig. 13. (b) Equivalent circuit with voltage source.

• 5.7. TRANSFORMER COUPLED TRANSISTOR AMPLIFIER

The R-C coupled amplifiers have low voltage and power gain. It is because the low resistance offered by the input of each stage to the preceding stage decreases the effective load resistance and hence the gain. If the effective load resistance of each stage could be increased, the voltage and power gain could be increased. This can be achieved by transformer coupling.

Circuit of two stage transformer-coupled transistor amplifier : Figure 14 shows the circuit of two stage transformer-coupled transistor amplifier. A coupling transformer is used to feed the output of one stage to the input of the next stage. In the circuit, T_1 is the coupling transformer whereas T_2 is the output transformer. C_1 is the input coupling capacitor whereas C_e's are by pass capacitors which apply signal between base and emitter. Resistors R_1 and R_2 are used to provide correct biasing while R_e's are the emitter stabilising resistors.

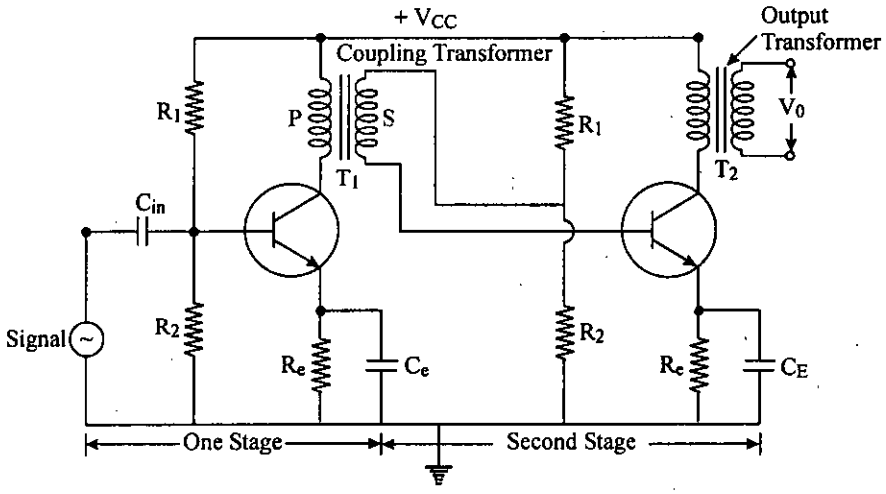


Fig. 14. Two stage transformer coupled amplifier.

Operation : When input signal is coupled through C_1 to the base of first transistor, it appears in an amplified form in the primary P of the coupling transformer. The voltage developed across the primary is transferred to the input of the next stage by transformer secondary. The secondary of T_1 applies the signal to the base of second

transistor which appears in an amplified form in the primary of output transformer T_2. The second stage works in an exactly similar manner.

Frequency response : The frequency response of a transformer-coupled amplifier is shown in figure 15.

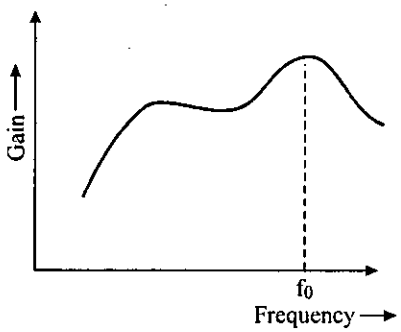


Fig. 15.

It is obvious from the figure that the frequency response is rather poor *i.e.,* gain is constant only over a small range of frequency. There is a decrease in the gain at low frequencies. This is because, the output voltage is equal to a.c. collector current multiplied by the reactance of the primary of coupling transformer.

At low frequencies, the reactance of primary begins to fall resulting in decreased gain. Again there is a decrease in the gain at high frequencies except for the resonant rise in gain at resonant frequency of the tuned circuit formed by the inductance and winding capacitance in the circuit. The distributed capacitance existing beween different turns of the winding acts as a bypass capacitor at high frequencies. This reduces the output voltage and hence the gain of the amplifier. Thus transformer coupled amplifier introduces frequency distortion due to disproportionate ampli- fication of frequencies in a complete signal such as music, speech etc.

The flat part of frequency response curve in transformer coupled amplifier is small as compared to the *R-C* coupled amplifier. It can be designed to have a flat frequency response curve over the entire audio frequency range, but the cost will be 10 to 20 times more than that of the *R-C* coupld amplifier.

Advantages : (i) There is no loss of signal power in collector or base resistors.

(ii) It provides a higher voltage gain.

(iii) An excellent impedance matching can be achieved in a transformer coupled amplifier. It is easy to make the inductive reactance of primary equal to the output impedance of the transistor and reactance of secondary equal to the input impedance of the next stage.

Disadvantages : (i) It has a poor frequency response.

(ii) It is bulky and costly particularly at audio frequencies because of its heavy iron core.

(iii) It produces hum in the outuput.

(iv) Frequency distribution is higher *i.e.,* low frequency signals are less amplified as compared to high frequency signals.

(v) At radio frequencies, the inductance and winding capacitance create a lot of problems.

Application : Transformer coupling is generally employed when the load is small. It is mostly used for power amplification and impedance matching.

• 5.8. A.C. EQUIVALENT CIRCUIT OF A FET

The complete a.c. equivalent circuit of a FET includes lead inductances, internal resistances, internal capacitance etc. However, in practice, the lead inductances are neglected. Figure 16 shows the equivalent FET circuit in Norton's form. On input side, C_{gd} and C_{gs} represent the capacitance between gate and drain capacitance between gate and source respectively. r_{gs} is the a.c. resistance from gate to source. On the output side, C_{ds} represents the capacitance between drain and source while r_{ds} is the a.c. resistance from drain to source.

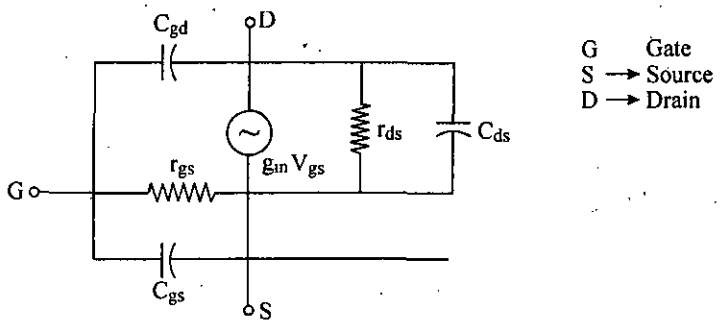


Fig. 16. a.c. equivalent circuit of a FET.

Low Frequency model : At low frequencies, all the capacitances become high enough to be neglected. The input resistance r_{gs} is infinite, as the reverse biased gate current is assumed to be zero. Similarly, the resistance between gate and drain is infinite. Thus the equivalent circuit for low frequencies, is shown in the figure 17. From the comparison of the low frequency model of FET with a low frequency h-parameter model of BJT, we note the following points :

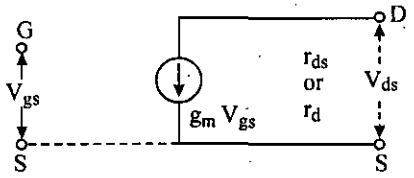


Fig. 17. Low frequency small signal model.

(a) Both have Norton's ouput circuit.

(b) In FET model, the generator current depends upon input voltage V_{gs} while in BJT model, the generator voltage depends upon input current.

(c) In case of FET, there is no feedback from output circuit to input circuit, while in case of BJT, the feedback takes place.

(d) The FET has almost infinite input resistance while the input resistance of a common emitter is about 1 KΩ.

The above facts show that low frequency FET forms a more ideal amplifier than conventional BJT.

High frequency model : At high frequencies, the capacitances between different nodes can not be neglected. The Fig. 18 shows the high frequency small signal model of FET. The capacitances show the following effects :

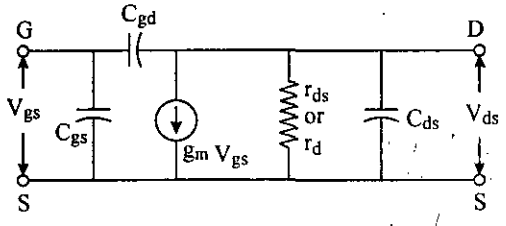


Fig. 18. High frequency small signal model.

(a) There is a feedback from output circuit to input circuit.

(b) Voltage gain drops rapidly as frequency increases.

• 5.9. COMMON SOURCE FET AMPLIFIER

Figure 19 shows the common source a.c. amplifier. In the figure, the drain current flows through R_S and develops a voltage which reverse biases the gate junction. R_G is provided for a d.c. return path. The Thevenin equivalent circuit for small signal common source amplifier is shown in Fig. 20. In this case $R_S = 0$ and the output V_0 is picked up at drain terminal D. The current I_D is given by

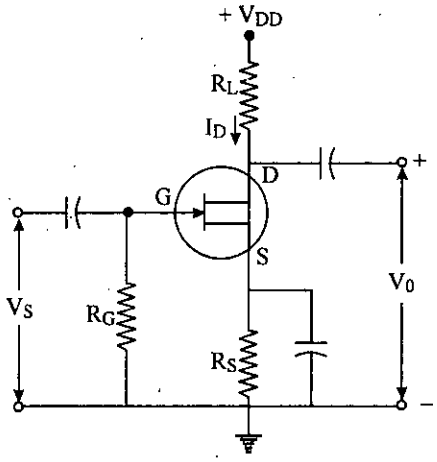


Fig. 19. Common source a.c. amplifier.

$$i_D = \frac{\mu V_i}{r_d + R_L}$$

The voltage V_0 developed across load R_L is given by

$$V_0 = -I_D \times R_L = \frac{-\mu V_i R_L}{r_d + R_L}$$

The negative sign indicates that the output voltage is out of phase with the input voltage. Now the voltage gain is given by

$$A_v = \frac{V_0}{V_i} = \frac{-\mu R_L}{r_d + R_L}$$

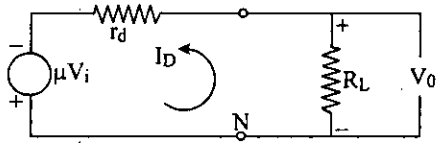


Fig. 20. Thevenin's equivalent circuit.

Output impedance (resistance) : The output resistance is a parallel combination of r_d and R_L which is given by $\frac{r_d R_L}{r_d + R_L}$.

Input impedance (resistance) : The input resistance is given by R_G.

• 5.10. COMMON DRAIN AMPLIFIER WITH A RESISTANCE IN THE DRAIN CIRCUITS

The basic circuit of a *P*-channel FET common drain or source follower is shown in figure 21.

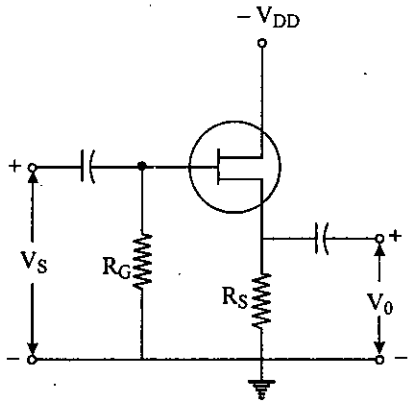


Fig. 21. Common drain amplifier or source follower.

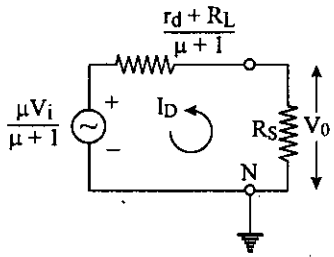


Fig. 22. Thevenin's equivalent circuit.

The low frequency of Thevenin's equivalent circuit with drain resistor R_L is shown in the figure 22. The current I_D can be shown equal to

$$I_D = \frac{\mu V_i}{r_d + R_L + (\mu + 1)R_S}$$

The output, in this case is taken across R_S

$$\therefore \quad V_0 = I_D R_S = \frac{\mu V_i R_S}{r_d + R_L + (\mu + 1)R_S}$$

$$= \frac{\mu/(\mu + 1)V_i R_S}{(r_d + R_L)/(\mu + 1) + R_S}$$

The voltage gain A_V is given by

$$A_V = \frac{V_0}{V_i} = \frac{\left(\frac{\mu}{\mu + 1}\right)R_S}{\left(\frac{r_d + R_L}{\mu + 1}\right) + R_S}$$

The output voltage is in phase with the input voltage. In case of a common drain amplifier $R_L = 0$ and output is picked up at source terminal. The voltage gain A_V is now given by

$$A_V = \frac{\left(\frac{\mu}{\mu + 1}\right)R_S}{\frac{r_d}{\mu + 1} + R_S}$$

or

$$A_V = \frac{\mu R_S}{r_d + (\mu + 1)R_S}$$

If $(\mu + 1)R_S >> r_d$, the voltage gain is

$$A_V = \frac{\mu}{\mu + 1}$$

For $\mu >> 1$, A_V is approximately equal to one. This signifis that the output voltage at the source follows the input voltage at the gate. This is why common drain amplifier is also known as **source follower.**

Output impedance (Resistance) : The output resistance is a parallel combination of R_S and $\frac{r_d}{\mu + 1}$.

Hence,

$$R_0 = \frac{R_S \times \frac{r_d}{\mu + 1}}{R_S + \frac{r_d}{\mu + 1}} = \frac{R_S \times r_d}{R_S(\mu + 1) + r_d}$$

$$= \frac{R_S \times r_d}{\mu R_S + r_d} \qquad \text{when } \mu >> 1$$

$$= \frac{R_S}{1 + g_m R_S} \qquad \text{since } \mu = r_d \times g_m$$

Input impedance (resistance) : The input resistance is determined by R_G.

Characteristics of a source follower : Following are the characteristics of a source follower FET.

(a) Voltage gain is less than unity.

(b) There is no phase reversal.

(c) Input impedance is high.

(d) Output impedance low.

• 5.11. FEEDBACK

The noise in the output of an amplifier is undesirable and must be kept to as small a level as possible. The noise level can be reduced considerably by feeding a fraction of output to the input signal. This is called **feedback.**

Feedback is a process in which a fraction of the output energy is combined with the input.

Depending upon whether the feedback energy aids are opposes the input signal, there are two basic types of feedback in amplifiers *viz.*, **positive feedback** and **negative feedback.**

(i) Positive feedback : When the feedback energy (voltage or current) is so applied that it increases the input energy *i.e.*, it is in phase with the input, it is called **positive feedback** or **regenerative** or **direct feedback.** Positive feedback increases gain of the amplifier. However, it has the disadvantage of increased distortion and instability. So positive feedback is seldom employed in amplifiers. If the positive feedback is sufficiently large, it leads to oscillations. and hence it is used in oscillators.

(ii) Negative feedback : When the feedback energy (voltage or current) is so applied that it decreases the input energy *i.e.*, it is out of phase with the input, it is called as **negative feedback** or **degenerative feedback** or **inverse feedback.** Negative feedback reduces gain of the amplifier. However, the advantages of negative feedback are : reduction in distortion, stability in gain, increased bandwidth and improved input and output impedances. So the negative feedback is frequently used in amplifiers.

Principle of negative feedback in amplifiers : A feedback amplifier has two parts *viz.*, an amplifier and feedback circuit which consists of resostors and returns a fraction of output energy back to the input. Let us consider a negative feedback amplifier shown in Fig. 23. The gain of the amplifier without feedback is *A*. Negative feedback is then applied by feeding a fraction *m* of the output voltage V_0 *i.e.*, mV_0 is the negative feedback applied back to the input of the amplifier. Therefore

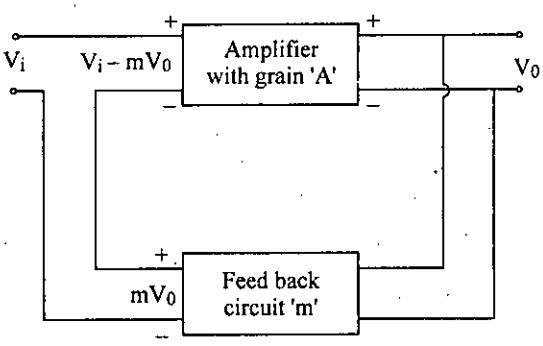


Fig. 23. Principle of negative feedback.

$$\text{Actual input to the amplifier} = V_i - mV_0'$$

This input is amplified A times by the amplifier and appears at the output as V_0 equal to $A(V_i - mV_0)$.

Fig. 23. Principle of negative feedback.

So $$A(V_i - mV_0) = V_0$$

or $$AV_i = V_0(1 + Am)$$

or $$\frac{V_0}{V_i} = \frac{A}{1 + Am}$$

This is voltage gain A' of the amplifier with negative feedback *i.e.*,

$$A' = \frac{A}{1 + Am}$$

It is obvious that the gain of the amplifier without feedback is reduced with the negative feedback by a factor $1 + Am$. The gain A is often called as **open loop gain** and the gain A' with feedback is known as closed loop gain (feedback loop is closed). m is the feedback fraction or ratio.

Advantages of negative feedback (reasons for negative feedback) : The following are the advantages of negative feedback in amplifiers :

(a) Gain stability : An important advantage of negative feedback is that the resultant gain of the amplifier is extremely stable.

The gain of the amplifier with negative feedback is given by

$$A' = \frac{A}{1 + Am}$$

The product Am is designed such that it is much greater than unity. Therefore, 1 may be neglected from the denominator. Hence,

$$A' = \frac{A}{Am} = \frac{1}{m}$$

Obviously the gain depends only on feedback ratio *i.e.,* characteristics of feedback circuit. As feedback circuit is usually a voltage divider (resistive network) and resistors can be selected very precisely with almost zero temperature coefficient of resistance, therefore, the gain is unaffected by changes in temperature, variations in transistor parameters and frequency. Hence the gain of the amplifier is extremely stable.

(b) Reduction in non-linear distortion : A large signal stage has non-linear distortion, as its voltage gain changes at various points in the cycle. The negative feedback reduces the non-linear distortion in large signal amplifiers. It can be proved mathematically that the distortion in amplifier with negative feedback D' is given by

$$D' = \frac{D}{1 + Am}$$

where D is the distortion without feedback.

Obviously, if the negative feedback is applied to an amplifier, the distortion is reduced by the factor $1 + Am$.

(c) Increase in band-width : The voltage gain of a negative feedback amplifier is independent of signal frequency *i.e.,* the gain of the amplifier is substantially constant over a wide range of frequency. Thus the band-width is increased and the frequency response of the amplifier is improved.

(d) Increase in input impedance : It can be shown that the input impedance Z'_{in} with negative feedback is given by

$$Z'_{in} = Z_{in} (1 + Am)$$

where Z_{in} is the input impedance without feedback. It is clear that by applying negative fedback, the input impedance of the amplifier is increased by a factor $1 + Am$ which is much greater than unity.

(e) Decrease in output impedance : It can be shown that the output impedance Z'_0 with negative feedback is given by

$$Z'_0 = \frac{Z_0}{1 + Am}$$

where Z_0 is the output impedance without feedback.

Obviously, the output impedance of a negative feedback amplifier decreases by a factor $1 + Am$.

With these changes in input and output impedances, the negative feedback amplifier can be made to serve the purpose of **impedance matching.**

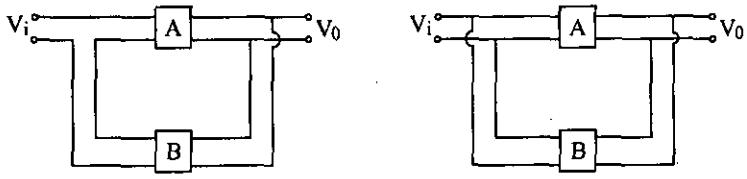
• 5.12. NEGATIVE FEEDBACK CIRCUITS

Negative feedback in an amplifier is a method for feeding a portion of the amplified output energy back to the input of the amplifier, so as to oppose the input signal. There are two types of negative feedback circuits (a) negative voltage feedback and (b) negative current feedback.

(a) Negative voltage feedback : In this method, the voltage feedback to the input of amplifier is proportional to the output voltage. This is further classified as :

(i) Voltage-series feedback [Figure 24 (i)]

(ii) Voltage-shunt feedback [Figure 24 (ii)]



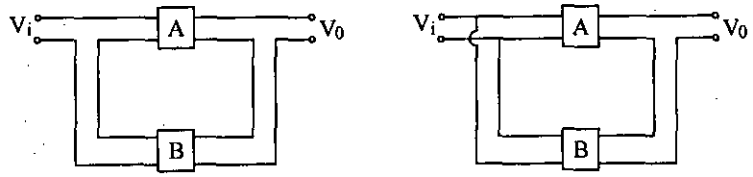
(i) Voltage-Series feedback (ii) Voltage-shunt feedback

Fig. 24. Negative voltage feedback.

(i) Voltage-series feedback : The amplifier circuit and feedback circuit are connected in series-parallel. The output voltage is combined in series with the input voltage via feedback. The feedback network shunts the output but is in series with the input. Hence output impedance decreases (parallel combination) while the input impedance increases (series combination) due to feedback.

(ii) Voltage-shunt feedback : Here a fraction of output voltage is combined with the input voltage in parallel (shunt). The feedback network shunts the output as well as the input. Hence both the input and output impedances decrease due to feedback.

Negative current feedback : In this method, the voltage feedback to the input of the amplifier is proportional to the output current. This is further classified as :



(i) Current-series feedback (ii) Voltage-shunt feedback

Fig. 25. Negative current feedback.

(i) Current-series feedback [Figure 25 (i)]

(ii) Current-shunt feedback [Figure 25 (ii)]

(i) Current series feedback : Here a part of the output current feeds back a proportional voltage in series with the input. The feedback network is in series with input as well as output and hence both the input and output impedances increase due to feedback.

(ii) Current shunt feedback : Here a part of output current feed-back a proportional voltage in parallel with the input voltage. The feedback network is in series with the output and in parallel with the input. Hence the output impedance is increased while the input impedance is decreased.

Emitter follower (An amplifier with negative current feedback) : *Figure 26 shows the circuit of an emitter follower. It differs from the circuitory of conventional amplifiers by the absence of collector load and emiter by-pass capacitor. The emitter resistance R_e itself acts as the load and the a.c. output voltage e_0 is taken across it. The biasing is usually provided by base-resistor method.*

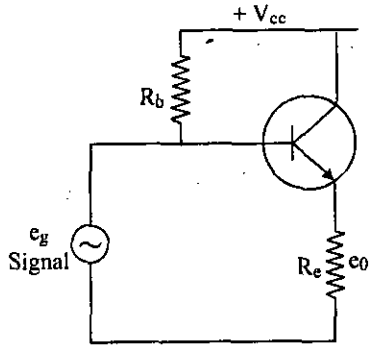


Fig. 26.

When signal e_s is applied, the resulting a.c. emitter current i_e, produces an output voltage $i_e R_e$ across emitter resistance. This voltage opposes the signal voltage, thus providing negative feedback. Obviously, it is a current feedback circuit, since the voltage feedback is proportional to the emitter current *i.e.*, output current. It is called **emitter follower** because voltage variations across base-emitter junction follow the emitter.

From the figure 26, the emitter current i_e is given by

$$i_e = -\frac{e_0}{R_e} \qquad \text{(the output is } -e_0\text{)}$$

$\therefore$ Base-emitter voltage

$$V_{be} = e_s - i_e R_e = e_s - \left(-\frac{e_0}{R_e}\right) R_e = e_s + e_0$$

Obviously, the feedback fraction $m = 1$ *i.e.*, feedback is 100%. Consequently, feedback voltage gain is nearly one. Similarly, it can be shown that current gain of emitter follower is less than unity.

The **principal features** of emitter follower are as follows :

(i) The gain is approximately unity.

(ii) The amplifier is non-phase inverting.

(iii) The input impedance is high.

(iv) The output impedance is low.

Due to these features, the emitter follower can be used, instead of transformer, for impedance matching. Emitter follower is not only more convenient than a transformer but it has much better frequency response *i.e.*, it works over a large frequency range.

• TEST YOURSELF

1. Classify the transistor amplifiers on the basis of their mode of operation ?

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2. Why is there a decrease in the gain at low frequenceies in a transformer coupled amplifier ?

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3. Give the expression to calculate the voltage gain of a transistor amplifier. Explain the symbols also.

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4. How does the voltage gain effect distortion of a signal ?

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5. Find out some applications of R-C coupled CE amplifer and explain why they are used there ?

.....

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• EXERCISE

1. What do you understand by single stage transistor amplifier ? Draw its circuit diagram and explain the function of each component and the various currents of the circuit.
2. Draw the d.c. and a.c. equivalent circuits of a transistor amplifier. Derive an expression for the voltage gain and power gain from its a.c. equivalent circuit.
3. What is phase reversal in a single stage common emitter transistor amplifier ? Show that the output voltage is 180° out of phase with the input voltage.

4. Describe the classification of transistor amplifiers.
5. Draw and describe the circuit of a two stage R.C. coupled CE amplifier. Sketch its frequency response curve and explain its behaviour at different frequency ranges.
6. Explain the working of a transformer coupled transistor amplifier. Discuss its frequency response curve.
7. Describe an a.c. equivalent circuit of a FET and dicuss its low frequency and high frequency small signal model.
8. Draw the circuit of a common source FET amplifier and its low frequency small signal equivalent circuit. Derive expression for its voltage gain, output impedance and input impedance.
9. Draw the circuit of a common drain amplifier with a resistance in the drain circuit. Derive the expression for voltage gain, output impedance and input impedance.
10. What do you mean by feedback ? Discuss the principles of negative feedback in amplifiers.
11. What are various negative feedback circuits ? Describe the action of emitter follower.
12. The phase difference between input and output voltage of a common emitter transistor amplifier is :
    (a) 0° (b) 90°
    (c) 180° (d) none of the above
13. The gain of coupled amplifiers :
    (a) decreases (b) increases
    (c) both the above (d) none of the above
14. If the voltage gain of an amplifier is hundred then its desibel gain is :
    (a) 10 db (b) 20 db
    (c) 30 db (d) 40 db
15. The gain in negative feedback amplifier is :
    (a) reduces (b) increases
    (c) remains same (d) none of the above
16. The distortion in negative amplifier is :
    (a) reduces (b) increases
    (c) remains same (d) none of the above
17. The band width in a negative feedback amplifier is :
    (a) decreases (b) increases
    (c) remains same (d) none of the above
18. Positive feedback is used in :
    (a) amplifiers (b) oscillators
    (c) both the above (d) none of the above
19. The current gain of an emitter follower is :
    (a) zero (b) less than one
    (c) one (d) greater than one

• ANSWERS

12. (c) **13.** (b) **14.** (d) **15.** (a) **16.** (a) **17.** (b) **18.** (b) **19.** (b)